

Berry DG15 Discrete/UMA Schematics Document

Arrandale

Intel PCH

2010-02-03

REV : A00

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
M96:DIS M96 platform installed
*VRAM_1G:VRAM 128M*16 installed*
Colay :Manual modify BOM

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

Berry

Rev

A00

Date: Wednesday, February 10, 2010

Sheet 1 of 92

Berry Block Diagram (Discrete/UMA co-lay)

Project code : 91.4HH01.001
PCB P/N : 48.4HH01.0SA
Revision : 09909-1

#OnMainBoard

1. Park-XT; 512MB
(64Mx16b*4)
Dell P/N: 9TGTN\$AA HYNIX
Dell P/N: C995R\$AA SAMSUNG
2. Park-XT; 1GB (128Mx16b*4)
Dell P/N: PXFYJ\$AA HYNIX
Dell P/N: C09DT\$AA SAMSUNG
(1 and 2 co-lay)

Clock Generator
SLG8SP585 7

VRAM
1GB/512MB
85, 86, 87, 88

DDR3
800MHz

AMD Graphic
Park-XT
(Discrete only)
80, 81, 82, 83, 84

Intel CPU
Arrandale
8, 9, 10, 11, 12, 13, 14

DDRIII 800/1066 Channel A

DDRIII Slot 0
800/1066 18

DDRIII 800/1066 Channel B

DDRIII Slot 1
800/1066 19

PCIe x16
(Discrete only)

FDI x4x2
(UMA only)

DMI x4

Discreet/UMA Co-lay

HDMI Level shifter 57

LVDS (Dual Channel)

RGB CRT

HDMI 57
LCD 54

CRT Board 77
Left Side: USB x 2

Bluetooth 73

CAMERA 54

Intel PCH HM57
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIe ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20, 21, 22, 23, 24, 25, 26, 27, 28

I/O Board Connector 76

Mini-Card 802.11a/b/g

10/100 NIC Realtek RTL8103T-VB

RJ45 CONN

ESATA/USB Combo

Mini-Card WWAN

SIM

Right Side: USB x 1

CardReader Realtek RTS5159 78

SD/MMC+/MS/MS Pro/xD

Azalia CODEC IDT 92HD79B1 30
Internal Analog MIC
HPI
MIC IN

2CH SPEAKER

Flash ROM 4MB 62

LPC debug port 70

HDD 59

ODD 59

KBC
NUVOTON NPCE781BA0DX 37

Flash ROM 256kB 62

Touch PAD 58

Int. KB 58

Thermal Main: G7922 Sec: EMC2102

Fan 58

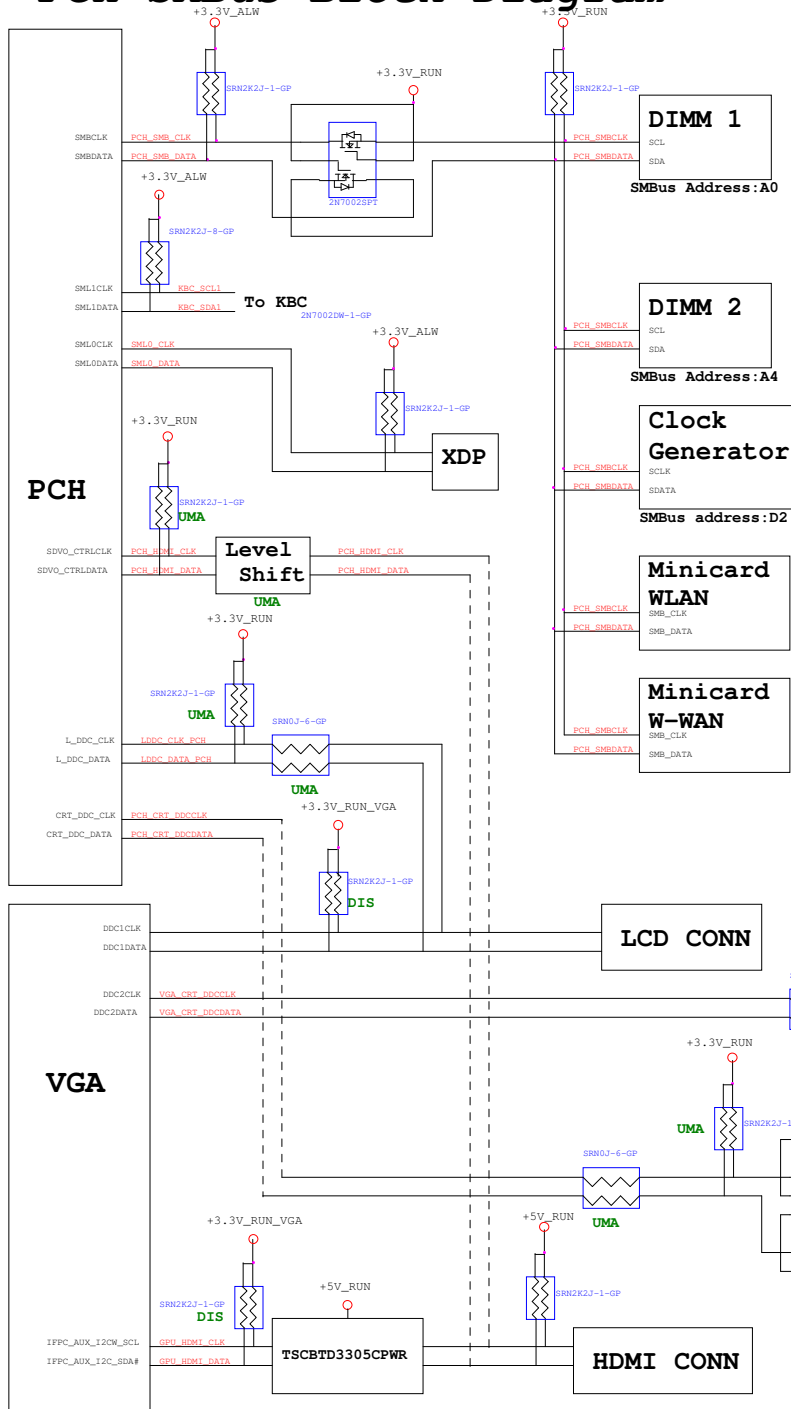
CPU DC/DC ISL62883 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT
SYSTEM DC/DC RT8205B 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW
SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
SYSTEM DC/DC TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE
VGA RT8208B 89	
INPUTS	OUTPUTS
+PWR_SRC	+VGA_CORE
TI CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_RUN_VGA
SYSTEM DC/DC APL5930 90	
INPUTS	OUTPUTS
+1.5V_SUS	+1.0V_RUN_VGA
Switches	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top L2: VCC L3: Signal L4: Signal L5: GND L6: Bottom	

<Core Design>

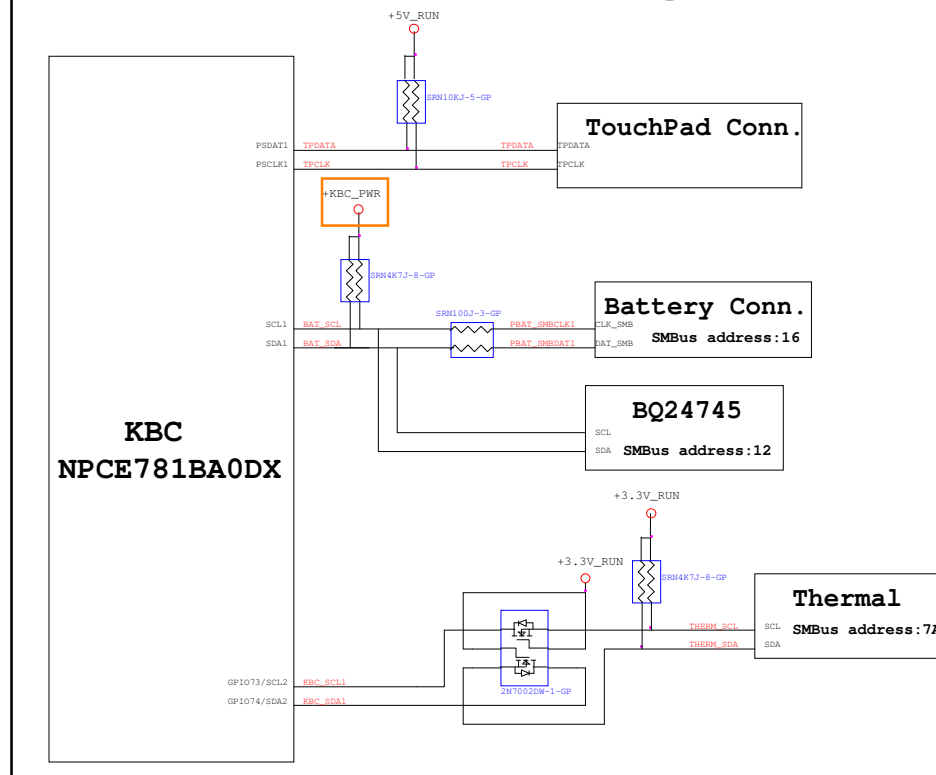
DELL	
Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Block Diagram	
Size A3	Document Number Berry
Date: Wednesday, February 10, 2010	Sheet 2 of 92

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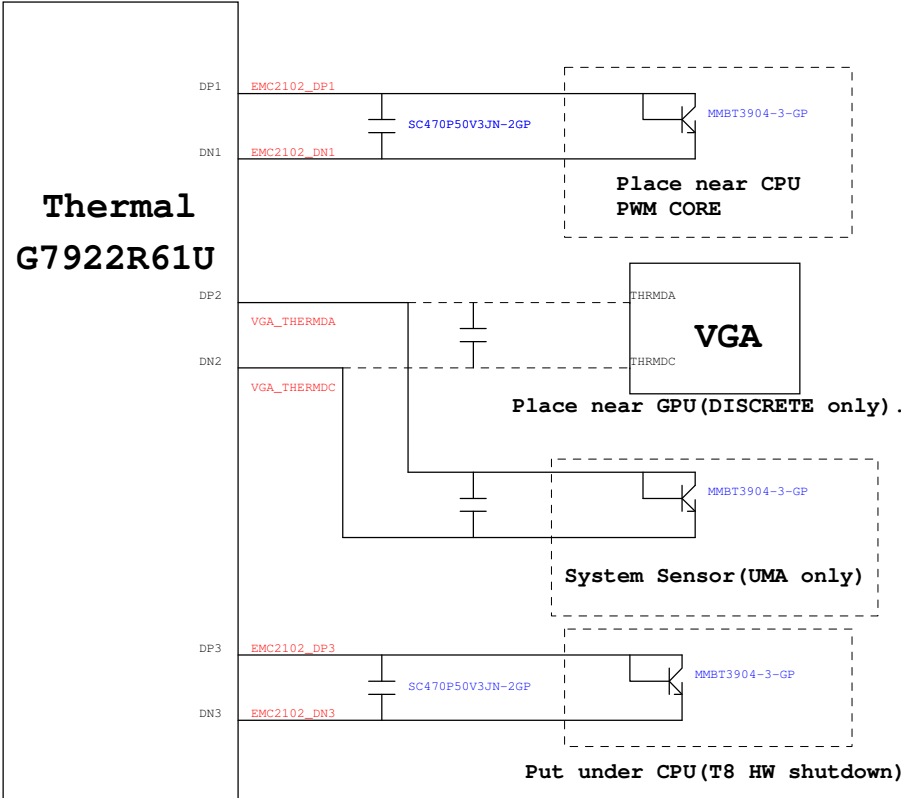
PCH SMBus Block Diagram



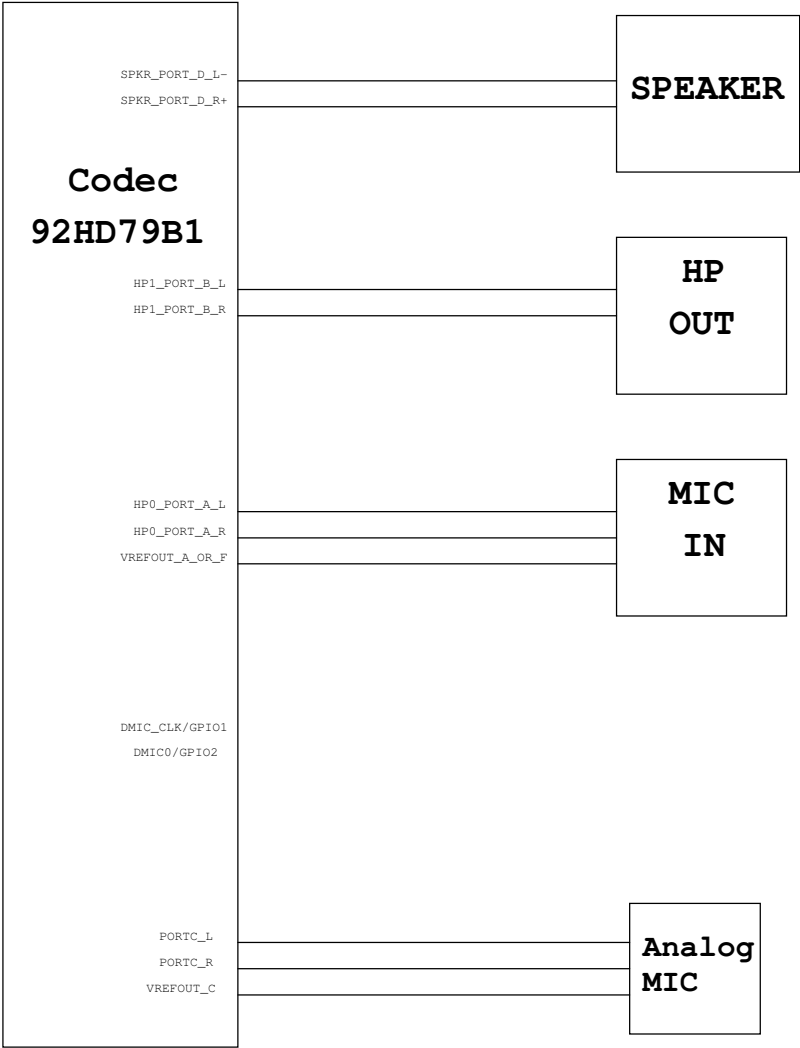
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1): Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	RESERVED
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	W-WAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	H55/HM55 no support
LANE8	H55/HM55 no support

USB Table

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	RESERVED
4	CARD READER
5	BLUETOOTH
6	HM55 no support
7	HM55 no support
8	USB1 (I/O Board)
9	USB0 (I/O Board ESATA)
10	RESERVED
11	W-WAN (I/O Board)
12	RESERVED
13	CAMERA

SATA Table


SATA	
Pair	Device
0	HDD
1	ODD
2	HM55 no support
3	HM55 no support
4	ESATA
5	RESERVED

Processor Strapping

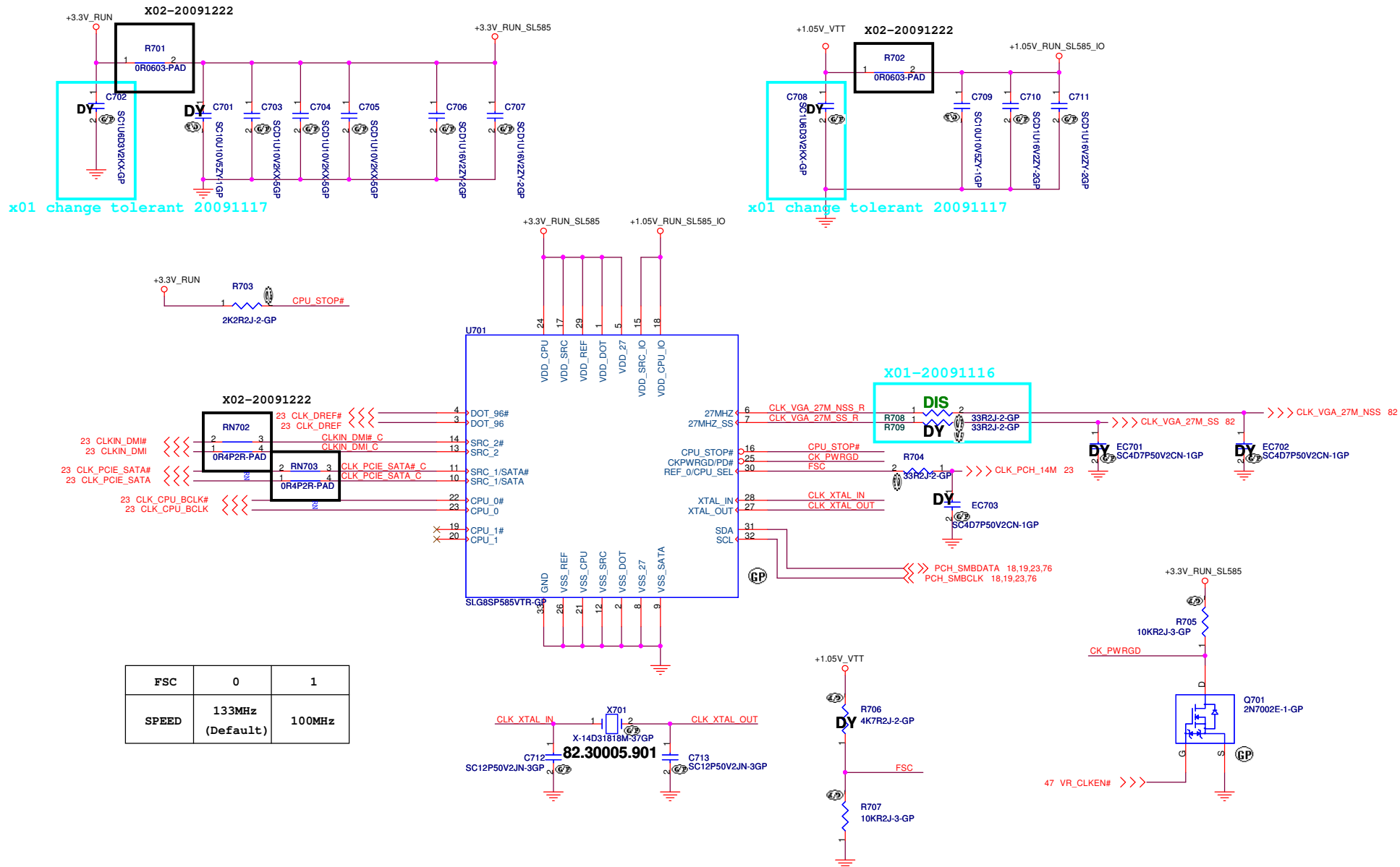
Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

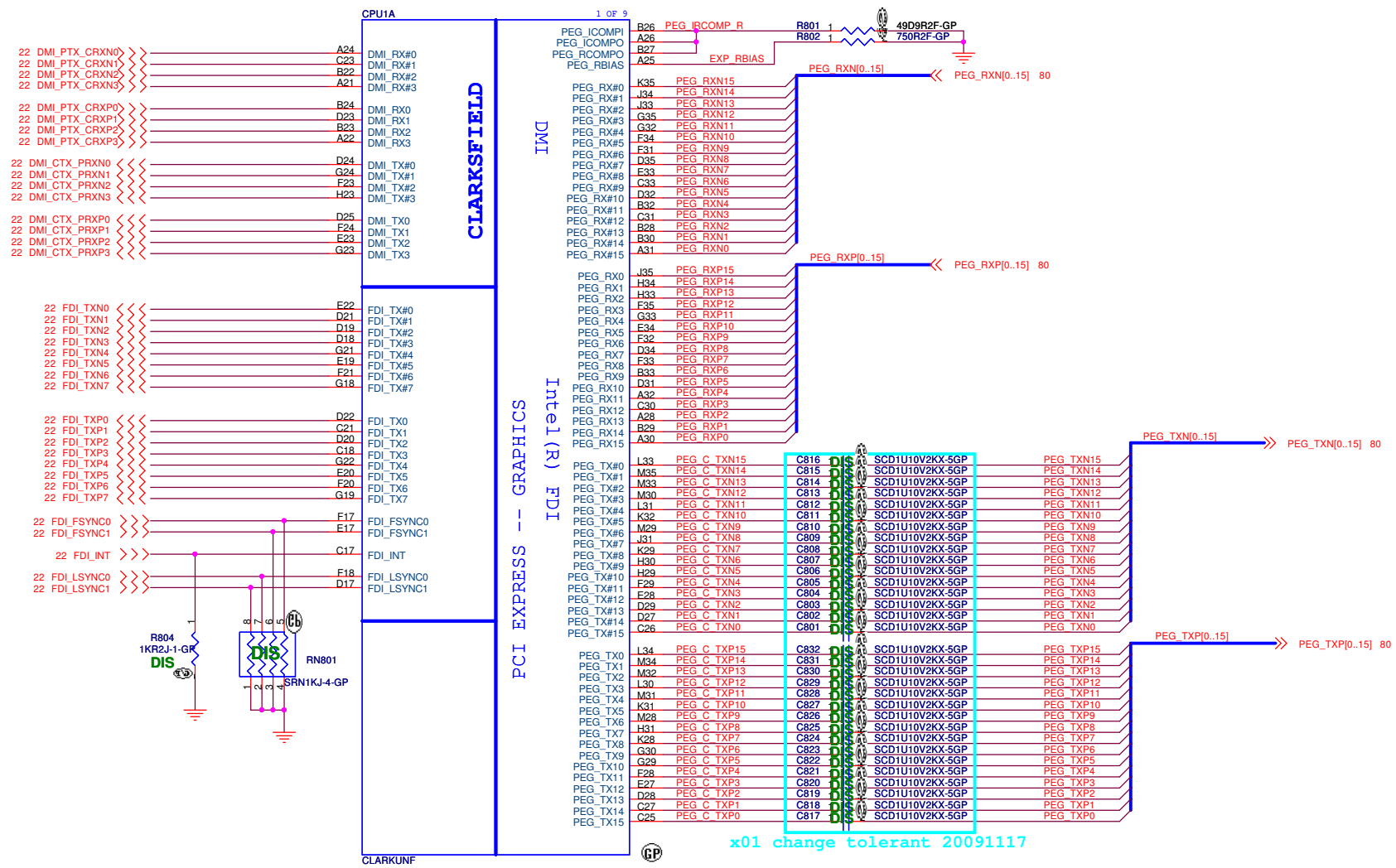
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Title			
<i>Table of Content</i>			
Size A3	Document Number Berry	Rev A00	
Date: Wednesday, February 10, 2010	Sheet 6	of	92

SSID = CLOCK



SSID = CPU



62.10055.341
SEC. 62.10053.561

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<Core Design>

DELL		Wistron Corporation	
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Title			
CPU (PCIE/DMI/FDI)			
Size	Document Number	Rev	A00
Berry			
Date: Monday, March 29, 2010	Sheet 8	of	92

SSID = CPU

18 M_A_DQ[63..0] <<>> M_A_DQ[63..0]

M_A_DQ0 A10 SA_DQ0
M_A_DQ1 C10 SA_DQ1
M_A_DQ2 A7 SA_DQ2
M_A_DQ3 B10 SA_DQ3
M_A_DQ4 B10 SA_DQ4
M_A_DQ5 D10 SA_DQ5
M_A_DQ6 E10 SA_DQ6
M_A_DQ7 A8 SA_DQ7
M_A_DQ8 D8 SA_DQ8
M_A_DQ9 F10 SA_DQ9
M_A_DQ10 E6 SA_DQ10
M_A_DQ11 E7 SA_DQ11
M_A_DQ12 E9 SA_DQ12
M_A_DQ13 B7 SA_DQ13
M_A_DQ14 E7 SA_DQ14
M_A_DQ15 C6 SA_DQ15
M_A_DQ16 H10 SA_DQ16
M_A_DQ17 G8 SA_DQ17
M_A_DQ18 K7 SA_DQ18
M_A_DQ19 J8 SA_DQ19
M_A_DQ20 G7 SA_DQ20
M_A_DQ21 G10 SA_DQ21
M_A_DQ22 J7 SA_DQ22
M_A_DQ23 J10 SA_DQ23
M_A_DQ24 L7 SA_DQ24
M_A_DQ25 M6 SA_DQ25
M_A_DQ26 M8 SA_DQ26
M_A_DQ27 L9 SA_DQ27
M_A_DQ28 L6 SA_DQ28
M_A_DQ29 L8 SA_DQ29
M_A_DQ30 N8 SA_DQ30
M_A_DQ31 P9 SA_DQ31
M_A_DQ32 AH5 SA_DQ32
M_A_DQ33 AE5 SA_DQ33
M_A_DQ34 AK6 SA_DQ34
M_A_DQ35 AK7 SA_DQ35
M_A_DQ36 AE6 SA_DQ36
M_A_DQ37 AG5 SA_DQ37
M_A_DQ38 AJ7 SA_DQ38
M_A_DQ39 AJ6 SA_DQ39
M_A_DQ40 AJ10 SA_DQ40
M_A_DQ41 AJ9 SA_DQ41
M_A_DQ42 AL10 SA_DQ42
M_A_DQ43 AK12 SA_DQ43
M_A_DQ44 AK8 SA_DQ44
M_A_DQ45 AL7 SA_DQ45
M_A_DQ46 AK11 SA_DQ46
M_A_DQ47 AL8 SA_DQ47
M_A_DQ48 AN8 SA_DQ48
M_A_DQ49 AN10 SA_DQ49
M_A_DQ50 AR11 SA_DQ50
M_A_DQ51 AL11 SA_DQ51
M_A_DQ52 AM9 SA_DQ52
M_A_DQ53 AN9 SA_DQ53
M_A_DQ54 AT11 SA_DQ54
M_A_DQ55 AP12 SA_DQ55
M_A_DQ56 AM12 SA_DQ56
M_A_DQ57 AN12 SA_DQ57
M_A_DQ58 AM13 SA_DQ58
M_A_DQ59 AT14 SA_DQ59
M_A_DQ60 AT12 SA_DQ60
M_A_DQ61 AL13 SA_DQ61
M_A_DQ62 AP14 SA_DQ62
M_A_DQ63 AP14 SA_DQ63

18 M_A_BS0 <<>> AC3 SA_BS0
18 M_A_BS1 <<>> AB2 SA_BS1
18 M_A_BS2 <<>> U7 SA_BS2

18 M_A_CAS# <<>> AE1C SA_CAS#
18 M_A_RAS# <<>> AB3C SA_RAS#
18 M_A_WE# <<>> AE3C SA_WE#

CLARKSFIELD

DDR SYSTEM MEMORY A

SA_CK0 AA6 <<>> M_CLK_DDR0 18
SA_CK#0 AA7 <<>> M_CLK_DDR#0 18
SA_CKE0 P7 <<>> M_CKE0 18

SA_CK1 Y6 <<>> M_CLK_DDR1 18
SA_CK#1 Y5 <<>> M_CLK_DDR#1 18
SA_CKE1 P6 <<>> M_CKE1 18

SA_CS#0 AE2 <<>> M_CS#0 18
SA_CS#1 AE8 <<>> M_CS#1 18

SA_ODT0 AD8 <<>> M_ODT0 18
SA_ODT1 AF9 <<>> M_ODT1 18

SA_DM0 B9 M_A_DM0
SA_DM1 D7 M_A_DM1
SA_DM2 H7 M_A_DM2
SA_DM3 M7 M_A_DM3
SA_DM4 AG6 M_A_DM4
SA_DM5 AM7 M_A_DM5
SA_DM6 AN10 M_A_DM6
SA_DM7 AN13 M_A_DM7

<<>> M_A_DM[7..0] 18

<<>> M_A_DQS#[7..0] 18

<<>> M_A_DQS[7..0] 18

<<>> M_A_A[15..0] 18

SA_DQS#0 C9 M_A_DQS#0
SA_DQS#1 F8 M_A_DQS#1
SA_DQS#2 B9 M_A_DQS#2
SA_DQS#3 AH7 M_A_DQS#3
SA_DQS#4 AK9 M_A_DQS#4
SA_DQS#5 AP11 M_A_DQS#5
SA_DQS#6 AT13 M_A_DQS#6
SA_DQS#7

SA_DQS0 C8 M_A_DQS0
SA_DQS1 F9 M_A_DQS1
SA_DQS2 H9 M_A_DQS2
SA_DQS3 M9 M_A_DQS3
SA_DQS4 AH8 M_A_DQS4
SA_DQS5 AK10 M_A_DQS5
SA_DQS6 AN11 M_A_DQS6
SA_DQS7 AR13 M_A_DQS7

SA_MA0 Y3 M_A_A0
SA_MA1 W1 M_A_A1
SA_MA2 AA8 M_A_A2
SA_MA3 AA9 M_A_A3
SA_MA4 V1 M_A_A4
SA_MA5 AA9 M_A_A5
SA_MA6 V8 M_A_A6
SA_MA7 T1 M_A_A7
SA_MA8 Y9 M_A_A8
SA_MA9 U6 M_A_A9
SA_MA10 AD4 M_A_A10
SA_MA11 T2 M_A_A11
SA_MA12 U3 M_A_A12
SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15



CLARKUNF

19 M_B_BS0 <<>> AB1 SB_BS0
19 M_B_BS1 <<>> W5 SB_BS1
19 M_B_BS2 <<>> R7 SB_BS2

19 M_B_CAS# <<>> AC5 SB_CAS#
19 M_B_RAS# <<>> Y7 SB_RAS#
19 M_B_WE# <<>> AC6 SB_WE#

M_B_DQ0 B5 SB_DQ0
M_B_DQ1 A5 SB_DQ1
M_B_DQ2 C3 SB_DQ2
M_B_DQ3 B3 SB_DQ3
M_B_DQ4 E4 SB_DQ4
M_B_DQ5 A4 SB_DQ5
M_B_DQ6 A4 SB_DQ6
M_B_DQ7 C4 SB_DQ7
M_B_DQ8 D1 SB_DQ8
M_B_DQ9 D2 SB_DQ9
M_B_DQ10 F2 SB_DQ10
M_B_DQ11 F1 SB_DQ11
M_B_DQ12 C2 SB_DQ12
M_B_DQ13 F5 SB_DQ13
M_B_DQ14 F3 SB_DQ14
M_B_DQ15 G4 SB_DQ15
M_B_DQ16 H6 SB_DQ16
M_B_DQ17 G2 SB_DQ17
M_B_DQ18 J6 SB_DQ18
M_B_DQ19 J3 SB_DQ19
M_B_DQ20 G1 SB_DQ20
M_B_DQ21 G5 SB_DQ21
M_B_DQ22 J2 SB_DQ22
M_B_DQ23 J1 SB_DQ23
M_B_DQ24 J5 SB_DQ24
M_B_DQ25 K2 SB_DQ25
M_B_DQ26 L3 SB_DQ26
M_B_DQ27 M1 SB_DQ27
M_B_DQ28 K5 SB_DQ28
M_B_DQ29 K4 SB_DQ29
M_B_DQ30 M4 SB_DQ30
M_B_DQ31 N5 SB_DQ31
M_B_DQ32 AF3 SB_DQ32
M_B_DQ33 AG1 SB_DQ33
M_B_DQ34 AJ3 SB_DQ34
M_B_DQ35 AK1 SB_DQ35
M_B_DQ36 AG4 SB_DQ36
M_B_DQ37 AG3 SB_DQ37
M_B_DQ38 AJ4 SB_DQ38
M_B_DQ39 AH4 SB_DQ39
M_B_DQ40 AK3 SB_DQ40
M_B_DQ41 AK4 SB_DQ41
M_B_DQ42 AM6 SB_DQ42
M_B_DQ43 AN2 SB_DQ43
M_B_DQ44 AK5 SB_DQ44
M_B_DQ45 AK2 SB_DQ45
M_B_DQ46 AM4 SB_DQ46
M_B_DQ47 AM3 SB_DQ47
M_B_DQ48 AP3 SB_DQ48
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M_B_DQ50 AT4 SB_DQ50
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M_B_DQ54 AT5 SB_DQ54
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M_B_DQ56 AN7 SB_DQ56
M_B_DQ57 AP6 SB_DQ57
M_B_DQ58 AP8 SB_DQ58
M_B_DQ59 AT9 SB_DQ59
M_B_DQ60 AT7 SB_DQ60
M_B_DQ61 AP9 SB_DQ61
M_B_DQ62 AR10 SB_DQ62
M_B_DQ63 AT10 SB_DQ63

CLARKSFIELD

DDR SYSTEM MEMORY - B

SB_CK0 W8 <<>> M_CLK_DDR2 19
SB_CK#0 W9 <<>> M_CLK_DDR#2 19
SB_CKE0 M3 <<>> M_CKE2 19

SB_CK1 V7 <<>> M_CLK_DDR3 19
SB_CK#1 V6 <<>> M_CLK_DDR#3 19
SB_CKE1 M2 <<>> M_CKE3 19

SB_CS#0 AB8 <<>> M_CS#2 19
SB_CS#1 AD6 <<>> M_CS#3 19

SB_ODT0 AC7 <<>> M_ODT2 19
SB_ODT1 AD1 <<>> M_ODT3 19

SB_DM0 D4 M_B_DM0
SB_DM1 E1 M_B_DM1
SB_DM2 H3 M_B_DM2
SB_DM3 K1 M_B_DM3
SB_DM4 AH1 M_B_DM4
SB_DM5 AL2 M_B_DM5
SB_DM6 AR4 M_B_DM6
SB_DM7 AT8 M_B_DM7

<<>> M_B_DM[7..0] 19

<<>> M_B_DQS#[7..0] 19

<<>> M_B_DQS[7..0] 19

<<>> M_B_A[15..0] 19

SB_DQS#0 D5 M_B_DQS#0
SB_DQS#1 F4 M_B_DQS#1
SB_DQS#2 J4 M_B_DQS#2
SB_DQS#3 L4 M_B_DQS#3
SB_DQS#4 AH2 M_B_DQS#4
SB_DQS#5 AL4 M_B_DQS#5
SB_DQS#6 AR5 M_B_DQS#6
SB_DQS#7 AR8 M_B_DQS#7

SB_DQS0 C5 M_B_DQS0
SB_DQS1 E3 M_B_DQS1
SB_DQS2 H4 M_B_DQS2
SB_DQS3 M5 M_B_DQS3
SB_DQS4 AG2 M_B_DQS4
SB_DQS5 AL5 M_B_DQS5
SB_DQS6 AP5 M_B_DQS6
SB_DQS7 AR7 M_B_DQS7

SB_MA0 U5 M_B_A0
SB_MA1 V2 M_B_A1
SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AE7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15



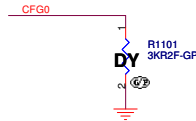
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DELL Wistron Corporation
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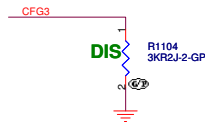
Title
Size Document Number
Date: Monday, March 29, 2010 Sheet 10 of 92
Rev A00
CPU (DDR)
Berry

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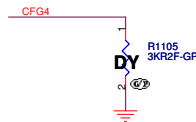
SSID = CPU



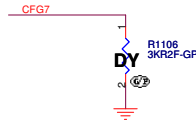
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



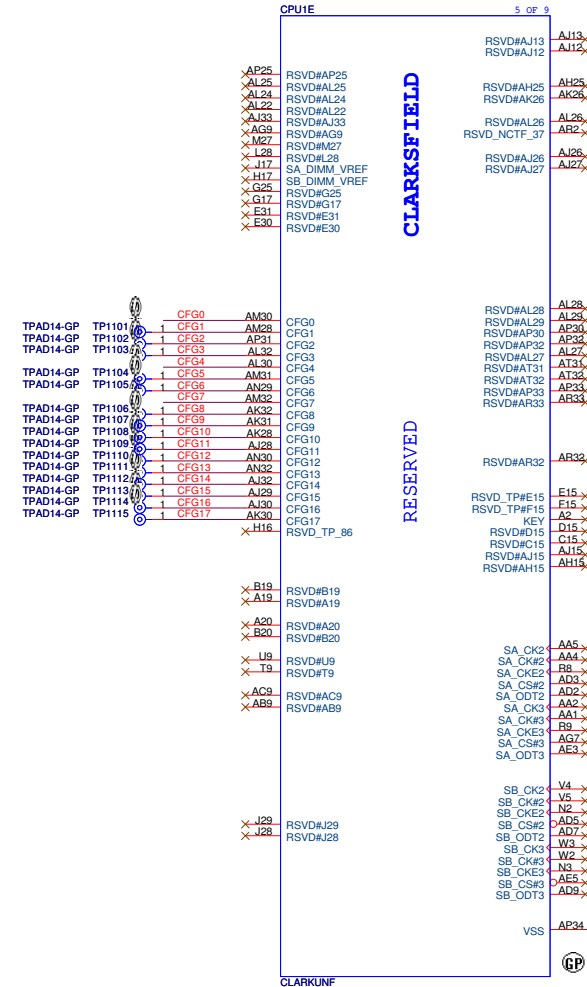
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



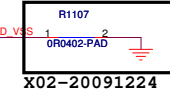
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



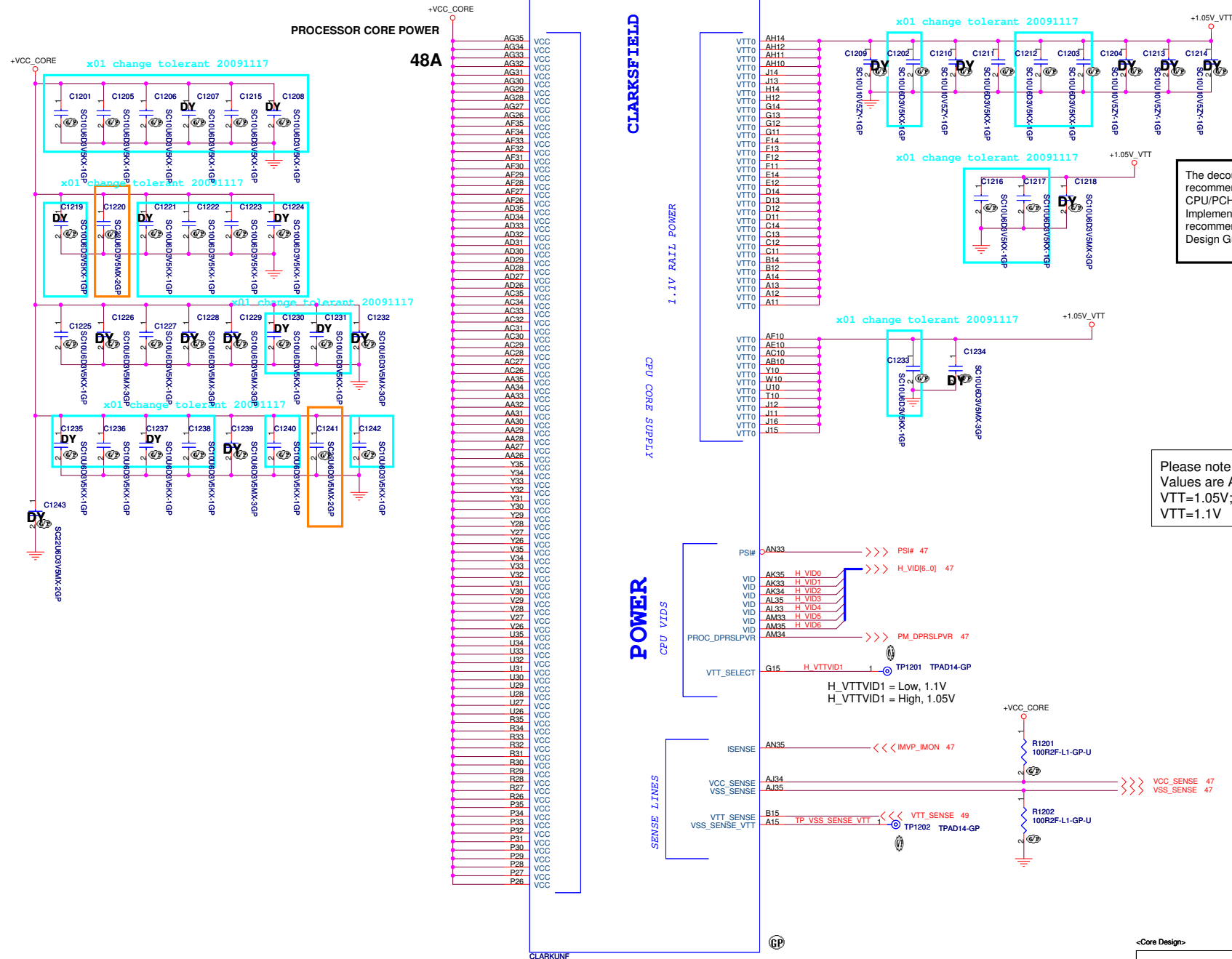
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Title			
CPU (RESERVED)			
Size	Document Number	Rev	A00
Date:	Wednesday, February 10, 2010	Sheet	11 of 92

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SSID = CPU



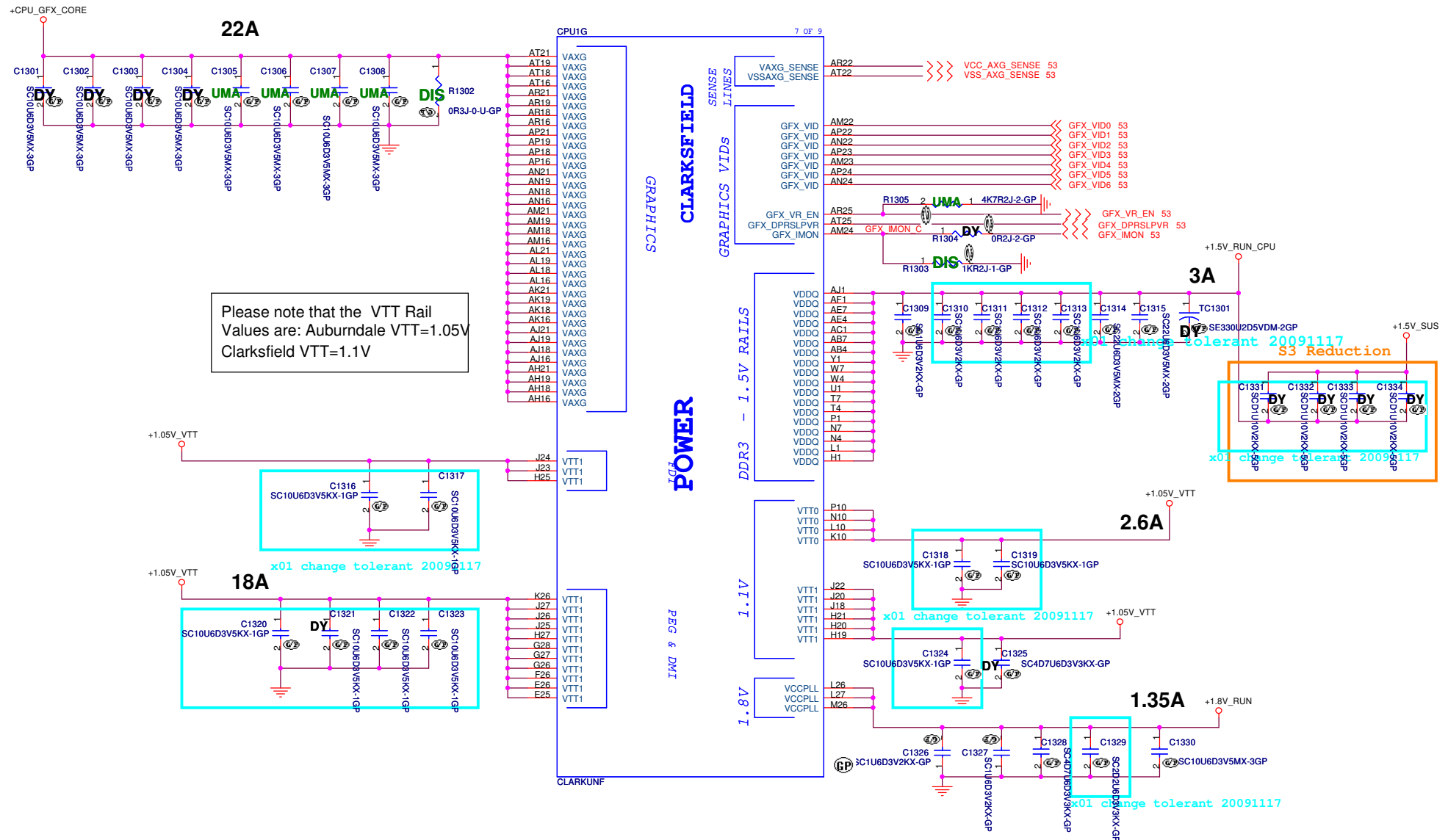
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarkfield VTT=1.1V

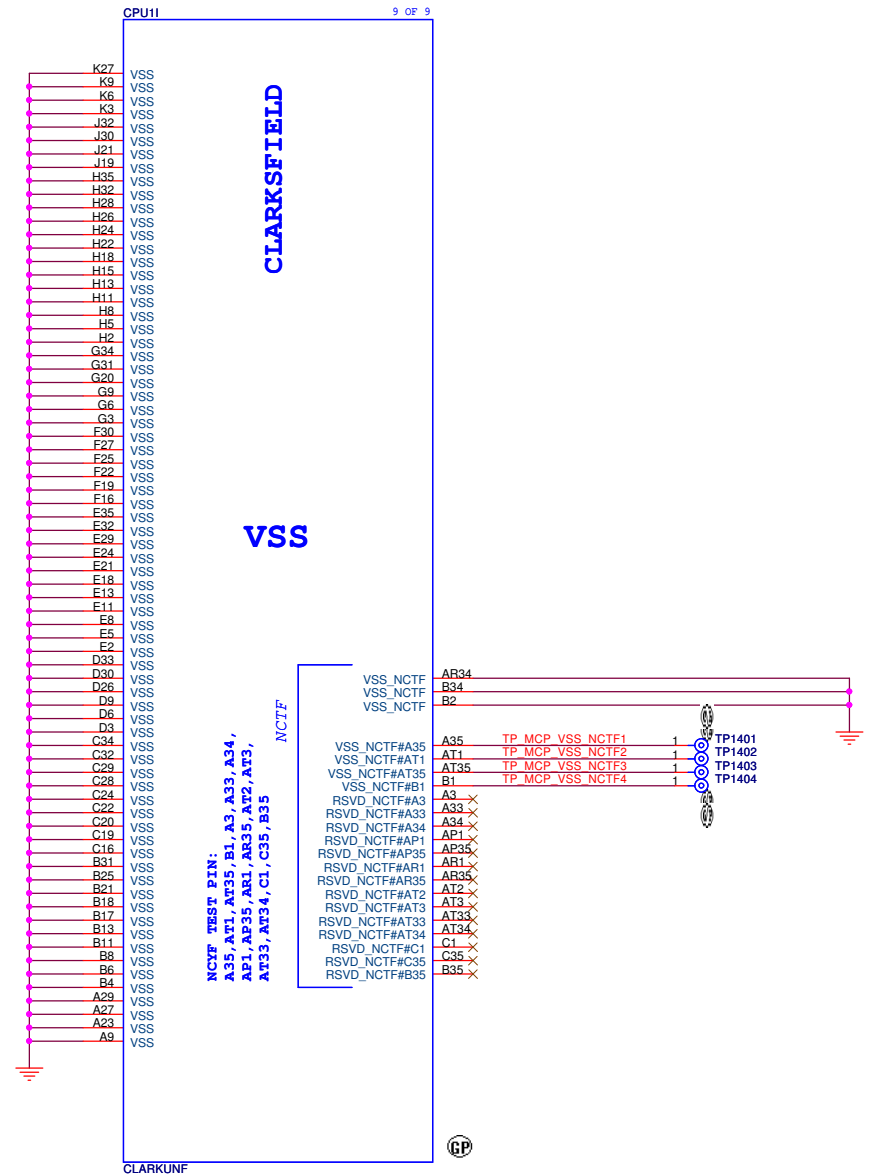
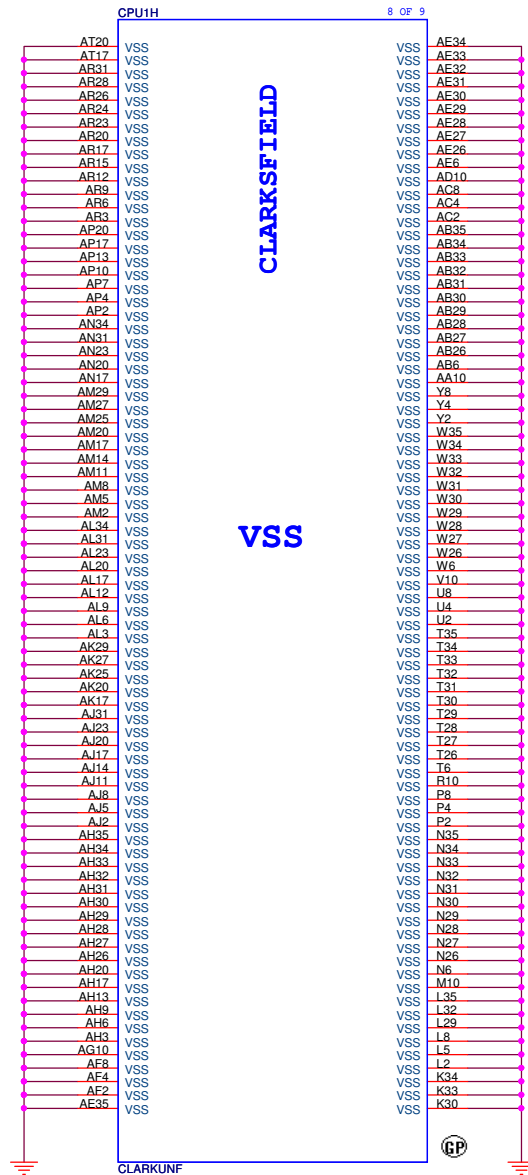
<Core Design>

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Title CPU (VCC_CORE)		
Size	Document Number Berry	Rev A00
Date: Monday, March 29, 2010	Sheet 12	of 92

SSID = CPU



SSID = CPU



<Core Design>




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Title			CPU (VSS)	
Size	Document Number		Rev	
	Berry		A00	
Date:	Wednesday, February 10, 2010	Sheet	14	of 92

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Size
A3

Document Number
Berry

Date: Wednesday, February 10, 2010


Rev
A00

Sheet 15 of 92

Reserved

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Reserved

Size A3	Document Number Berry	Rev A00
Date: Wednesday, February 10, 2010		Sheet 16 of 92

(Blanking)

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Title

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Document Number
Berry

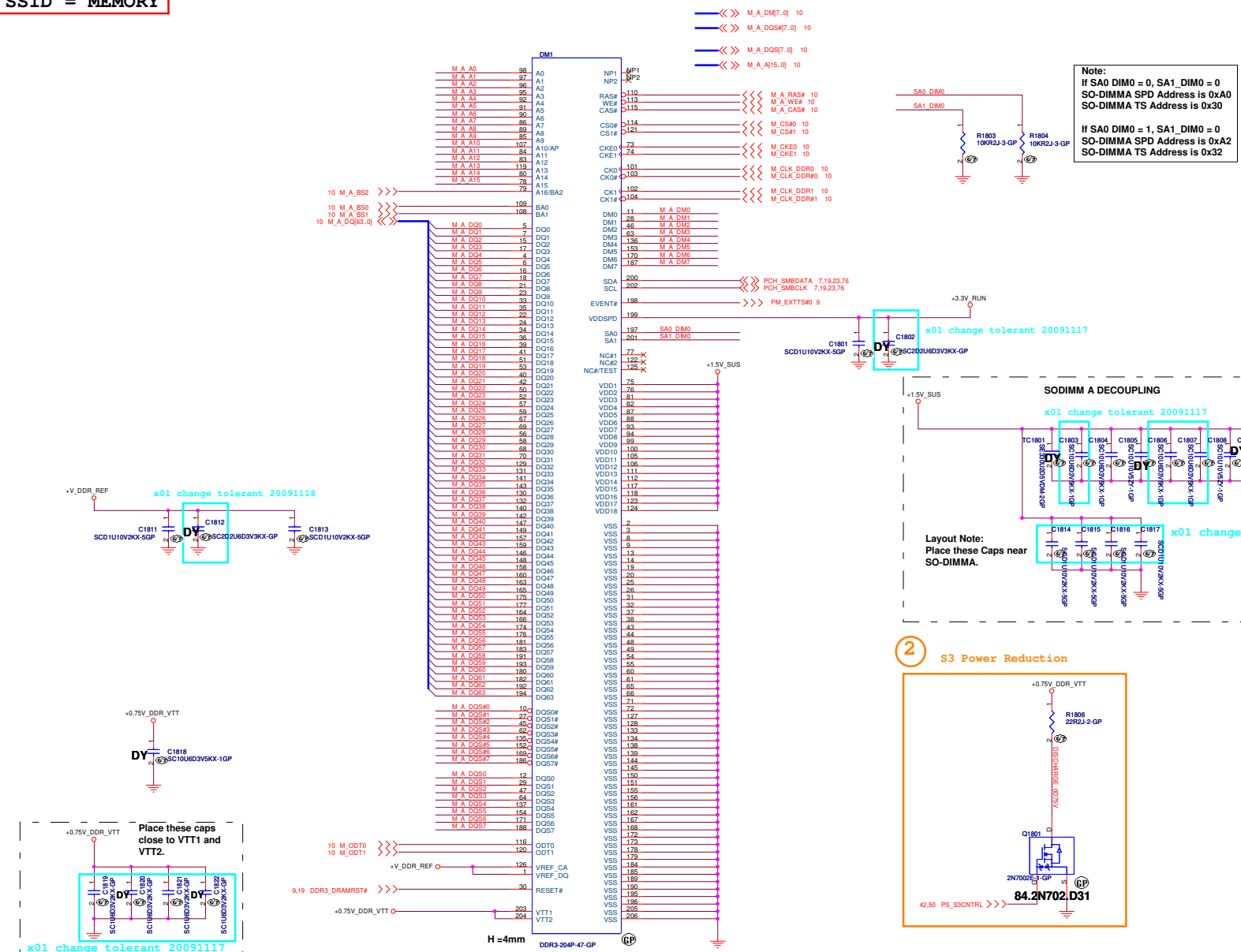
Date: Wednesday, February 10, 2010

Rev
A00

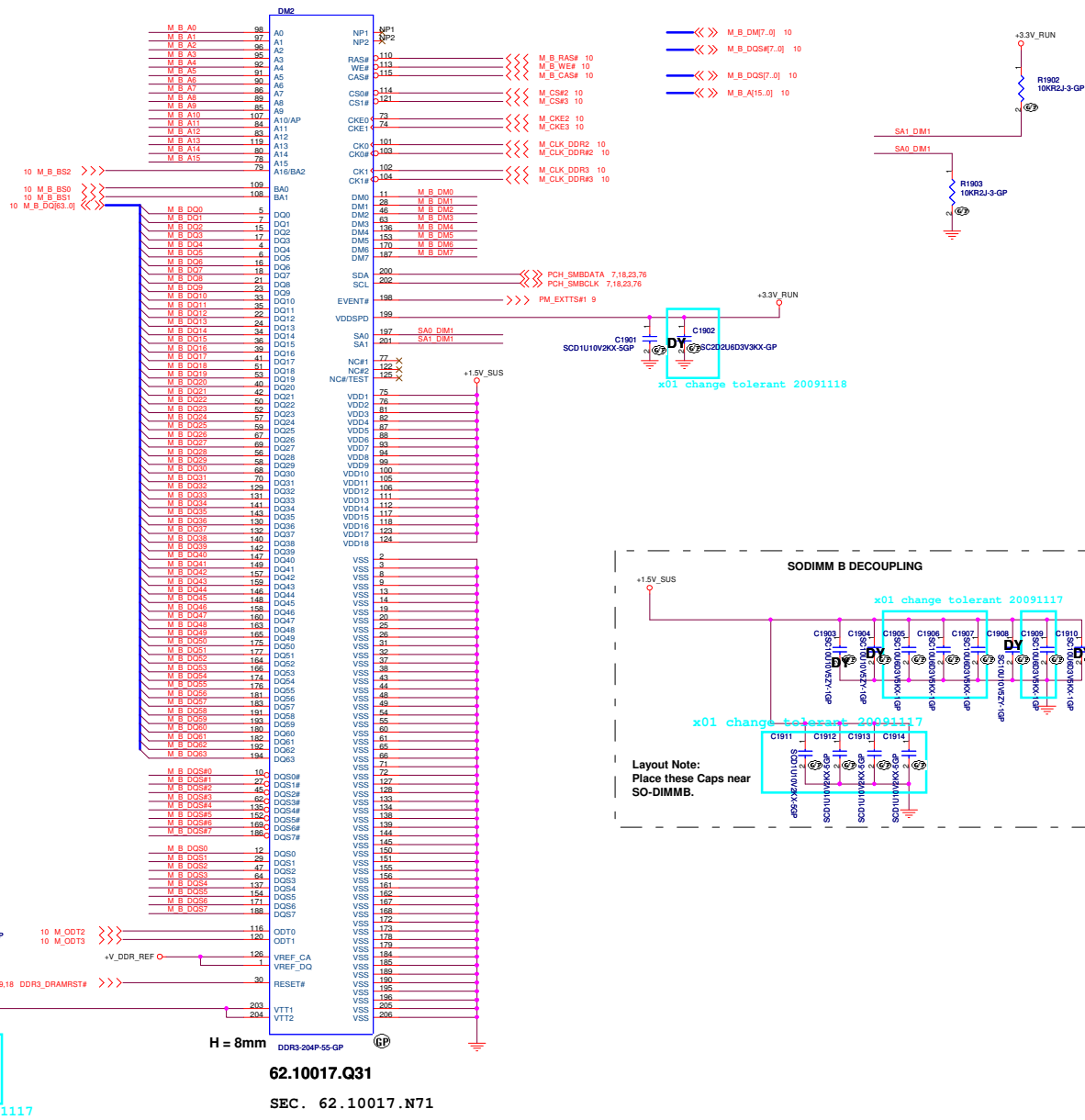
Sheet 17 of 92

Reserved

SSID = MEMORY

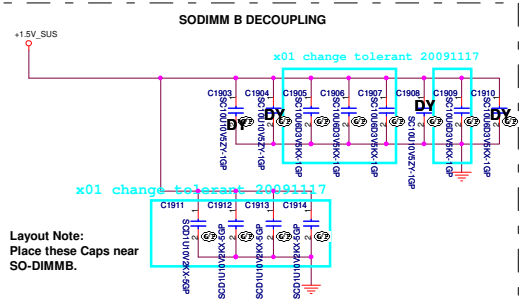


SSID = MEMORY



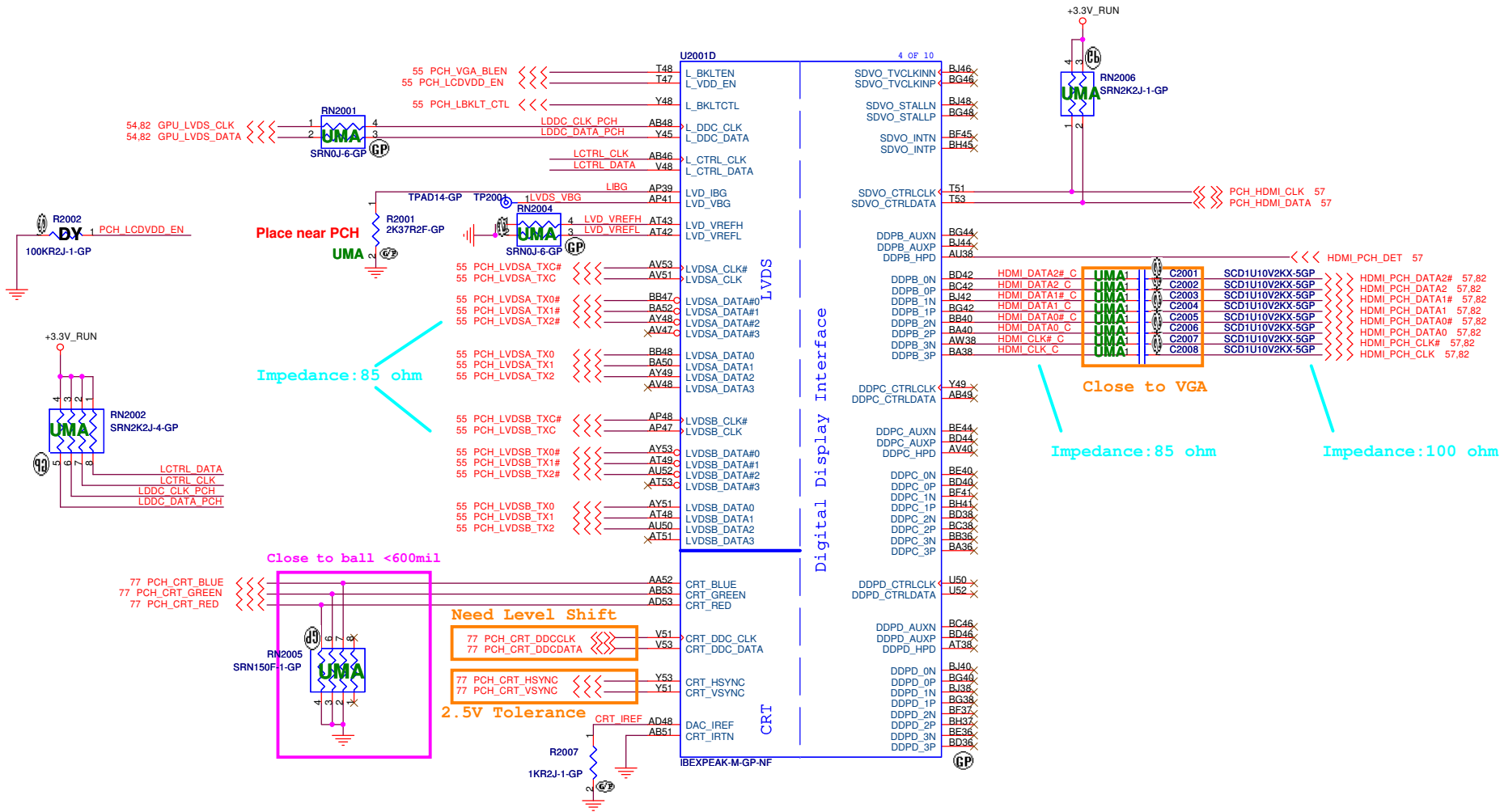
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

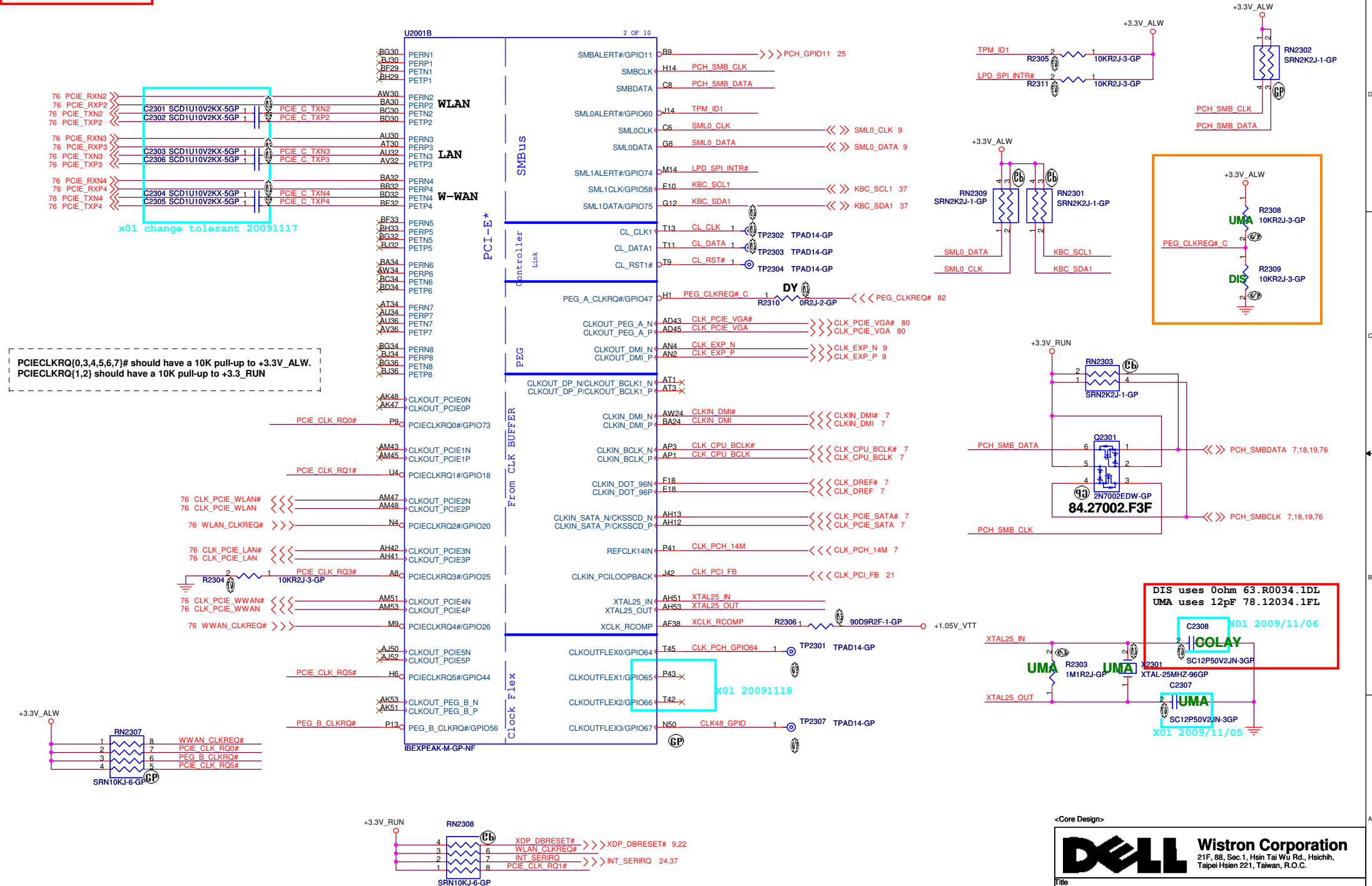
SO-DIMMB is placed farther from
the Processor than SO-DIMMA



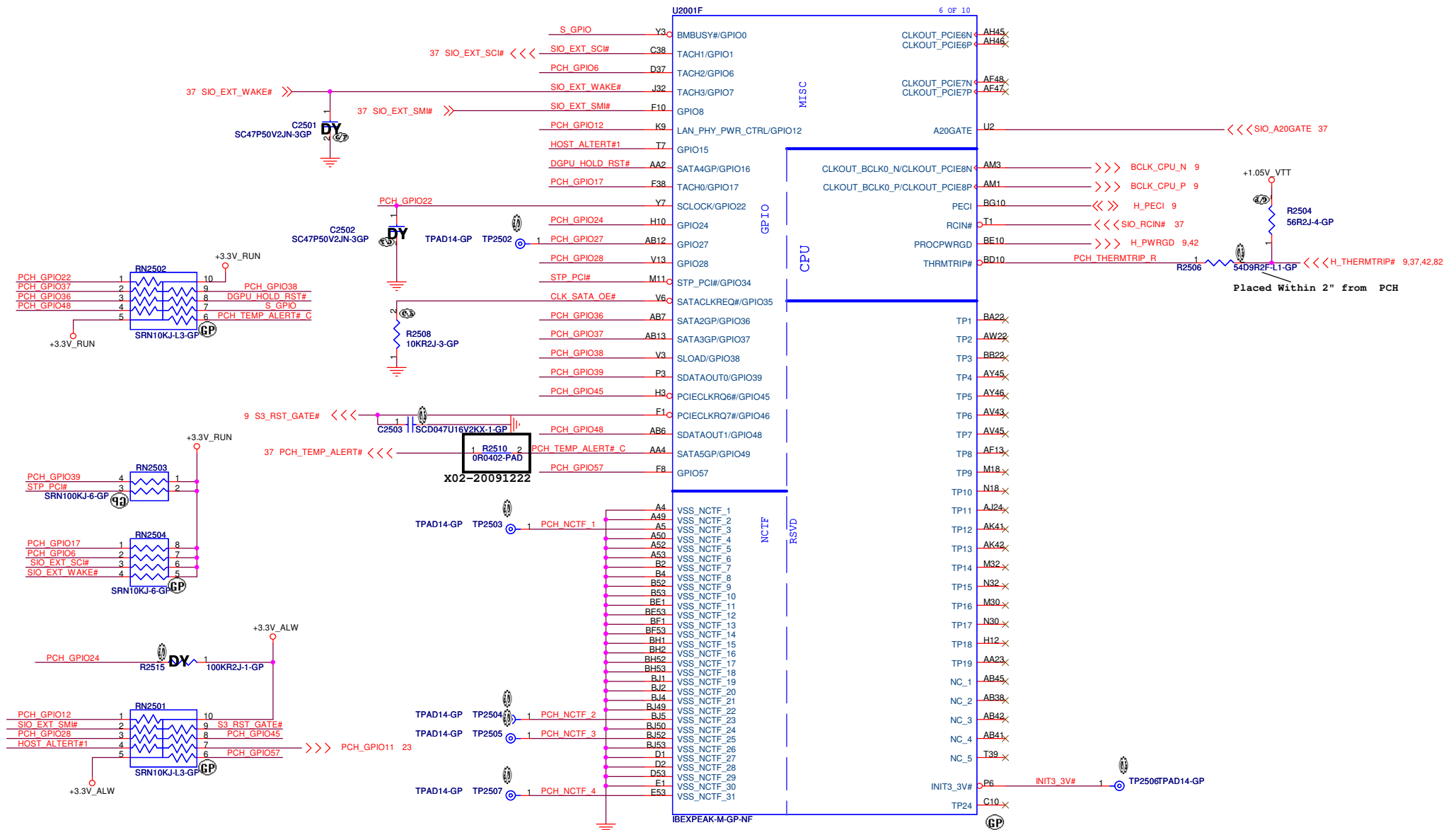
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PCH (LVDS/CRT/DDI)			
Size	Document Number Berry		Rev A00
Date: Monday, March 29, 2010	Sheet 20	of 92	

SSID = PCH



SSID = PCH



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Title

PCH (GPIO/CPU)

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Document Number

Berry

Rev	
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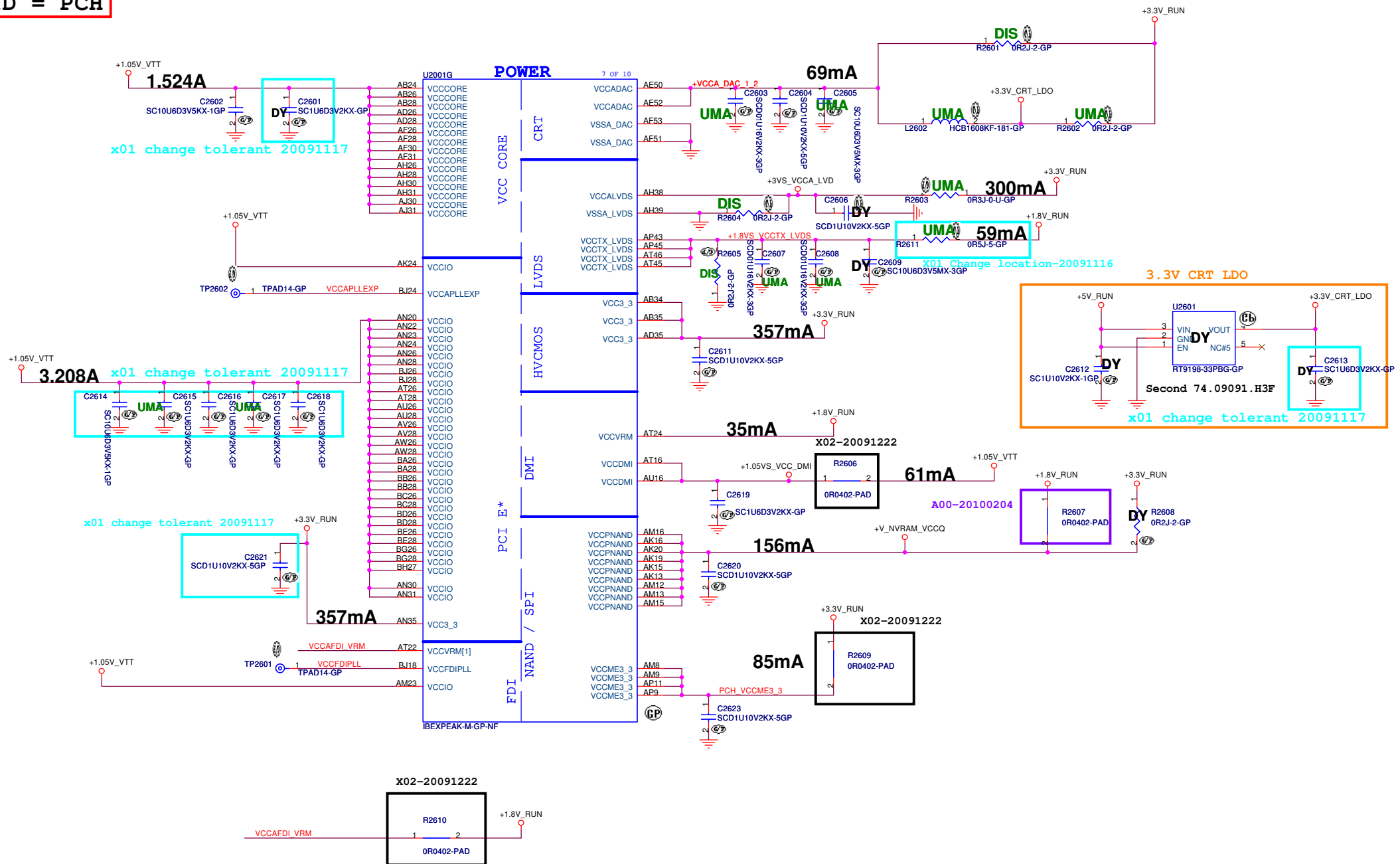
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Date: Monday, March 29, 2010

Sheet 25 of 92

<http://act.hntr.com>

SSID = PCH



<Core Design>



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Title	Author	Date	Location	Notes
1	John Doe	1998	New York	First entry
2	Jane Smith	2001	London	Second entry
3	Bob Johnson	2005	Paris	Third entry
4	Alice Brown	2010	Tokyo	Fourth entry
5	Charlie Davis	2015	Sydney	Fifth entry
6	Diana Prince	2020	Auckland	Sixth entry
7	Ethan Hunt	2025	Wellington	Seventh entry
8	Fiona Glenanne	2030	Christchurch	Eighth entry
9	Gavin Hastings	2035	Dunedin	Ninth entry
10	Helen Mirren	2040	Invercargill	Tenth entry

PCH (POWER1)

Size

Document Number

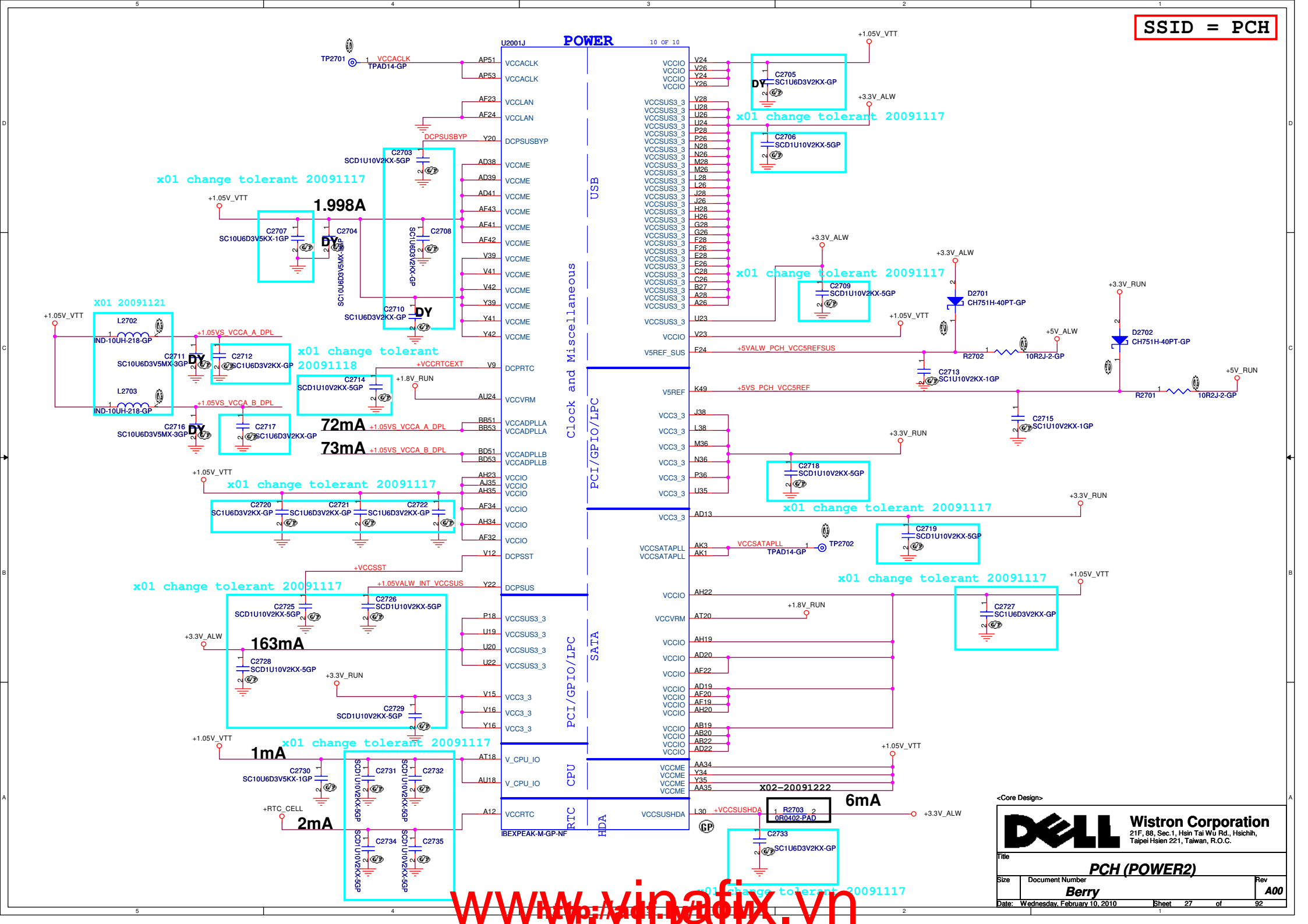
Size Document Number
Berry

Berry

Date: Wednesday, February 10, 2010

Sheet 26 of 92

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SSID = PCH



<Core Design>

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Title: **PCH (VSS)**

Size: Document Number: **Berry** Rev: **A00**

Date: Wednesday, February 10, 2010 Sheet 28 of 92

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Title

Size
A3

Document Number
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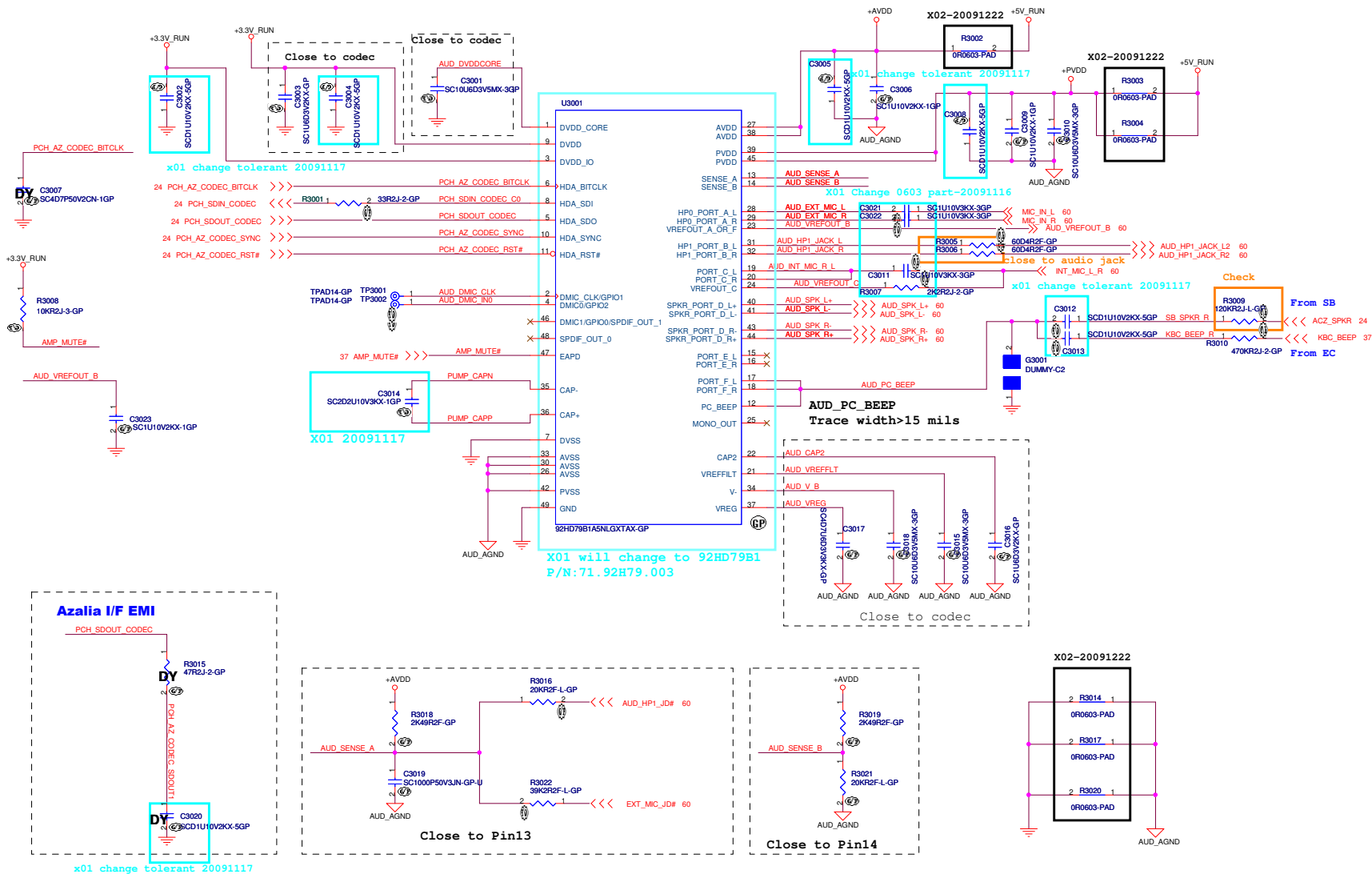
Date: Wednesday, February 10, 2010

Rev
A00

Sheet 29 of 92

Reserved

SSID = AUDIO



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Title				Audio Codec 92HD81B1			
Size	Document Number						Rev
Custom							A00
Berry							
Date:	Monday, March 23, 2010			Sheet	30	of	92

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Title

Size
A3

Document Number
Berry

Date: Wednesday, February 10, 2010

Rev
A00


Sheet 31 of 92

Reserved

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Title

Size
A3

Document Number
Berry

Date: Wednesday, February 10, 2010


Rev
A00

Sheet 33 of 92

Reserved

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<Core Design>



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Title

Reserved

Size A3	Document Number Berry	Rev A00
Date: Wednesday, February 10, 2010	Sheet 34 of 92	

(Blanking)

<Core Design>



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Title

Size
A3

Document Number
Berry

Date: Wednesday, February 10, 2010


Rev
A00

Sheet 35 of 92

Reserved

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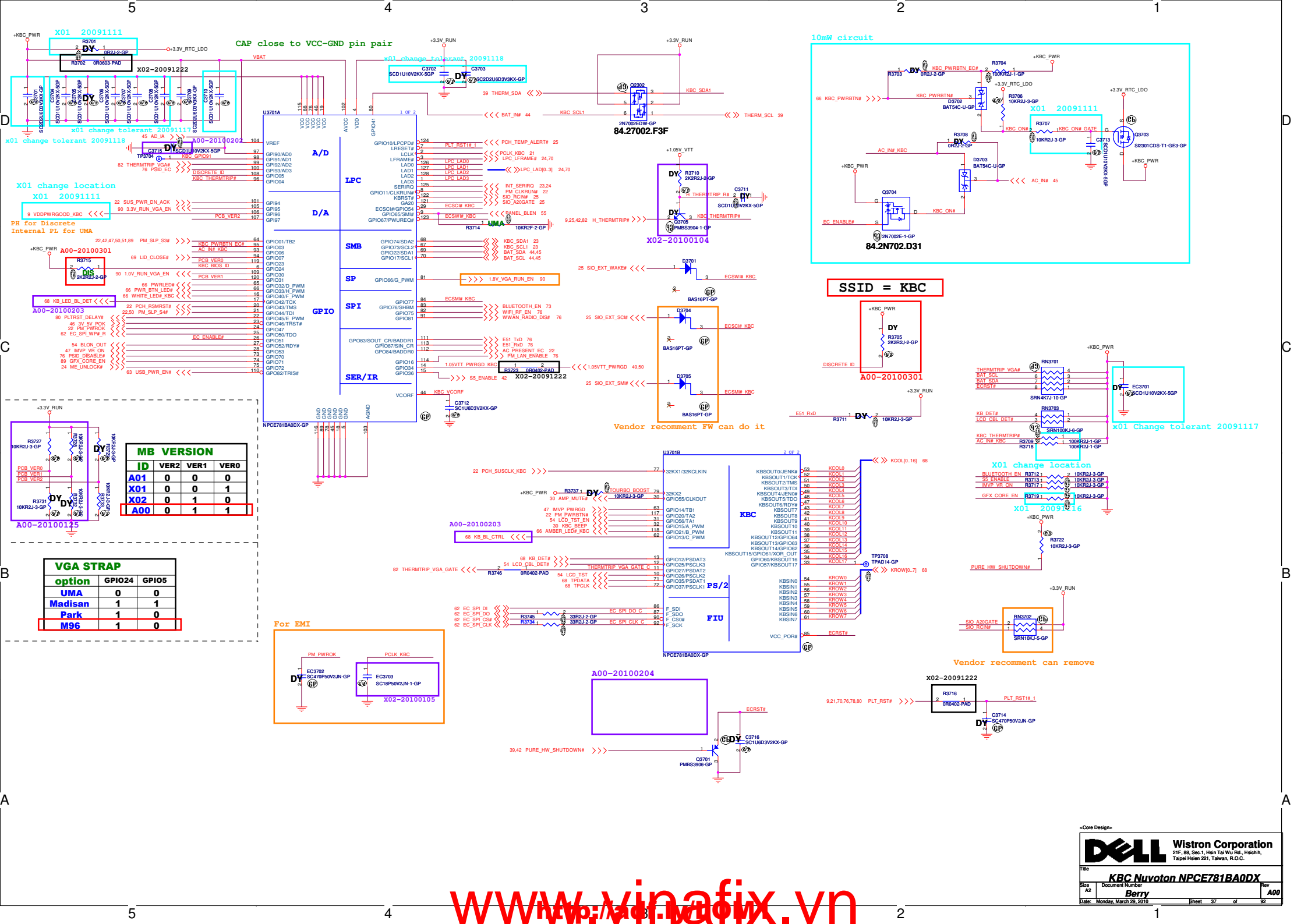


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Title

Reserved

Size A3	Document Number Berry	Rev A00
Date: Wednesday, February 10, 2010	Sheet 36 of 92	



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Title

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Size
A4

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Berry

Rev
A00

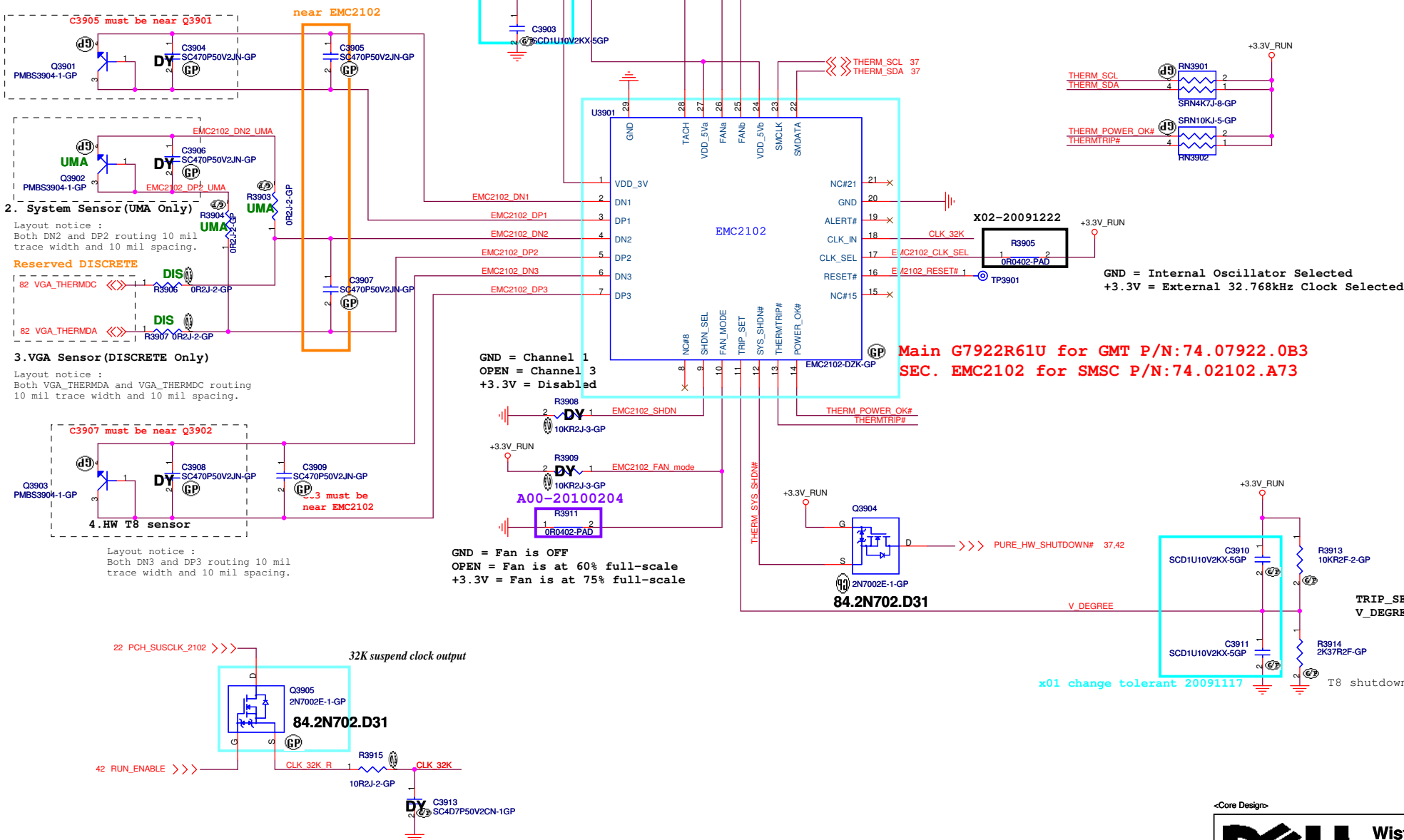
Date: Wednesday, February 10, 2010

Sheet 38 of 92

SSID = Thermal

1. Place near CPU PWM CORE and PCH.

Layout notice :
Both DN1 and DP1 routing 10 mil
trace width and 10 mil spacing.



<Core Design>




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Title			
<i>Thermal/Fan Controllor EMC2102</i>			
Size	Document Number	Rev	
Custom	<i>Berry</i>	<i>A00</i>	
Date:	Tuesday, April 06, 2010	Sheet 39 of	92

<http://addiction.vr>

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Title

Reserved

Size A3	Document Number Berry	Rev A00
Date: Wednesday, February 10, 2010	Sheet 40 of 92	

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Size
A3

Document Number
Berry

Date: Wednesday, February 10, 2010


Rev
A00

Sheet 41 of 92

Reserved

(Blanking)

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Size
A3

Document Number
Berry

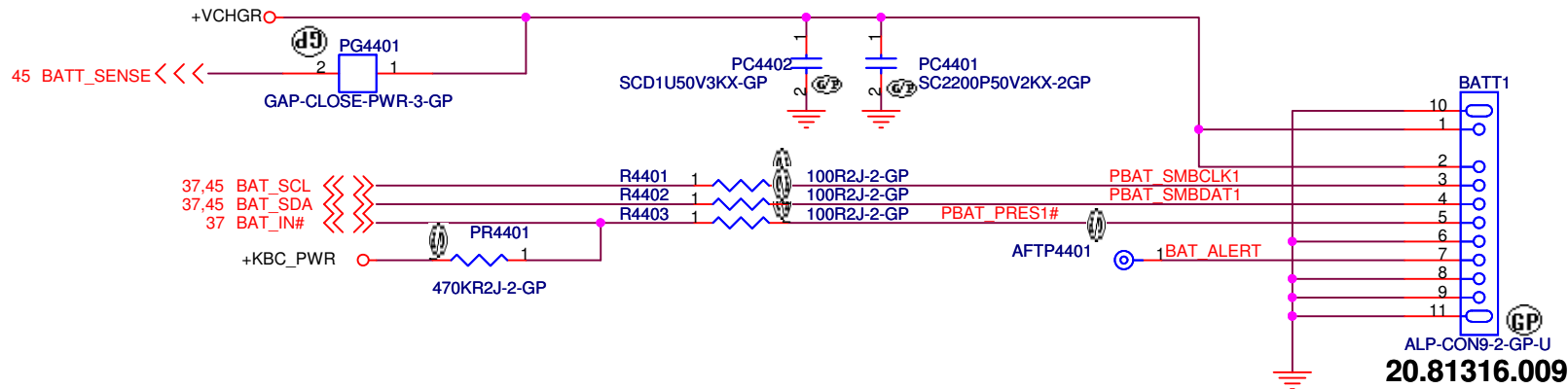
Date: Wednesday, February 10, 2010

Rev
A00

Sheet 43 of 92

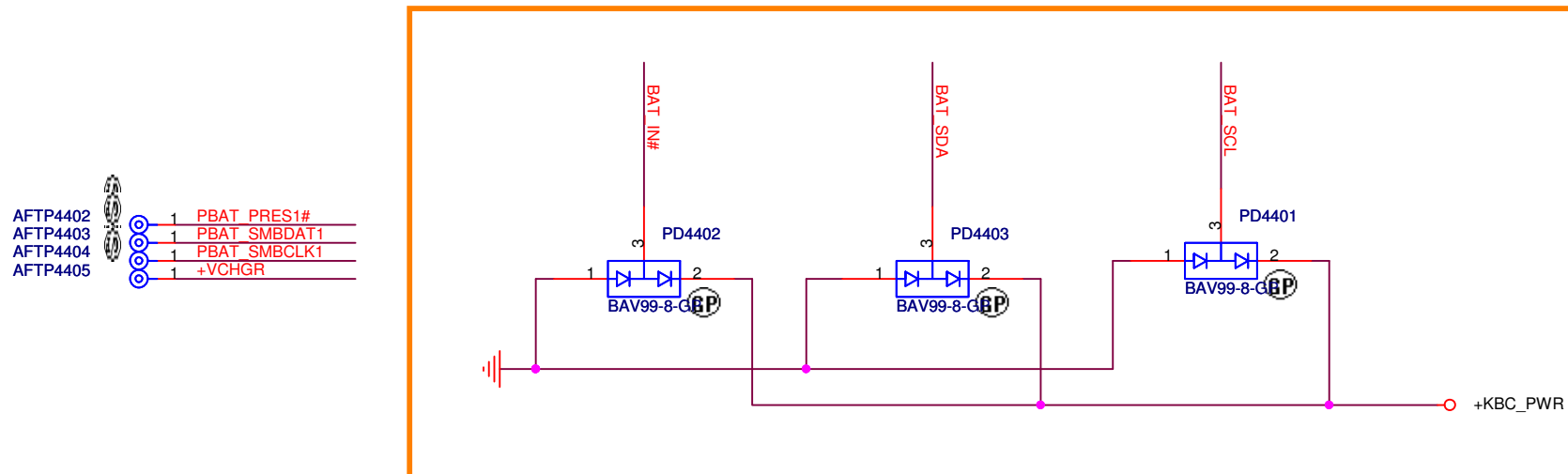
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Batt Connector



For actual location, need to be swap all pin

Close to Batt Connector



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Title

BATT CONN

Size
A4

Document Number

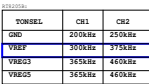
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Rev

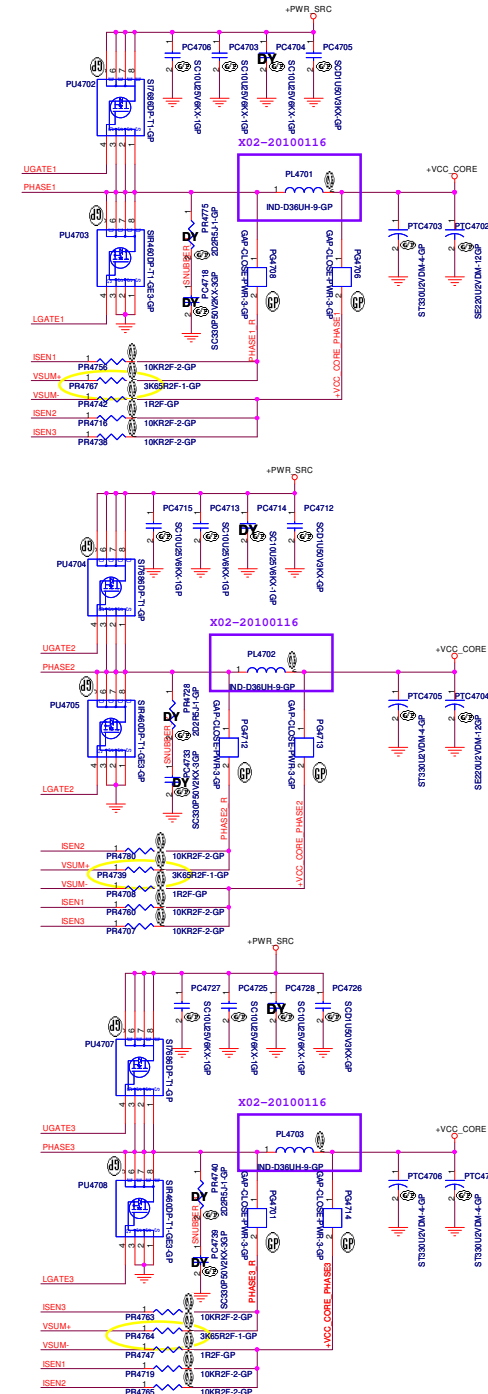
A00

Date: Monday, March 29, 2010

Sheet 44 of 92




 Wistron Corporation 21/F, 808, Sec. 1, Hsin Tai Wu Rd., Hsuehlin, Taipei Hsien 221, Taiwan, R.O.C.	
File	
RT8205B 5V/3D3V	
Size	Document Number
A1	Berry
Rev	A00
Date	Month
Monday	March 20, 2002
Board	48
of	92



<http://adefix.vn>

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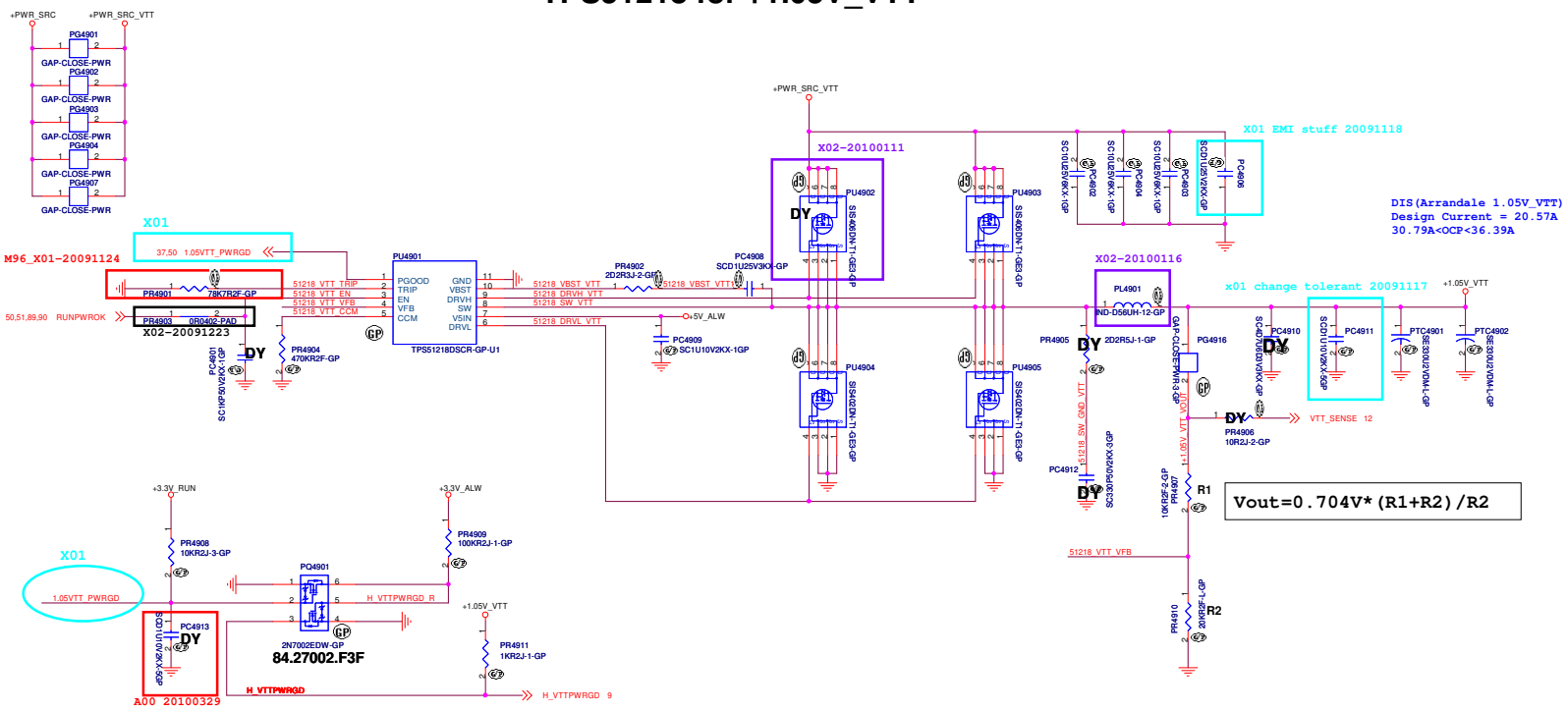
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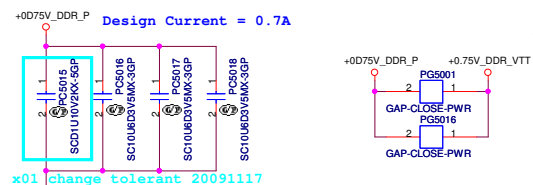
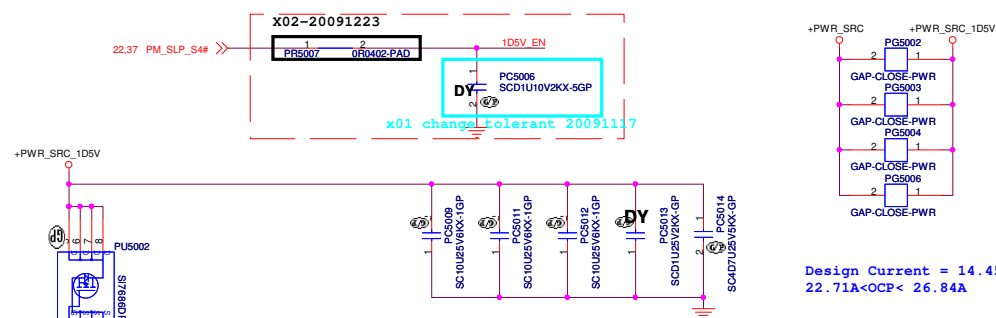
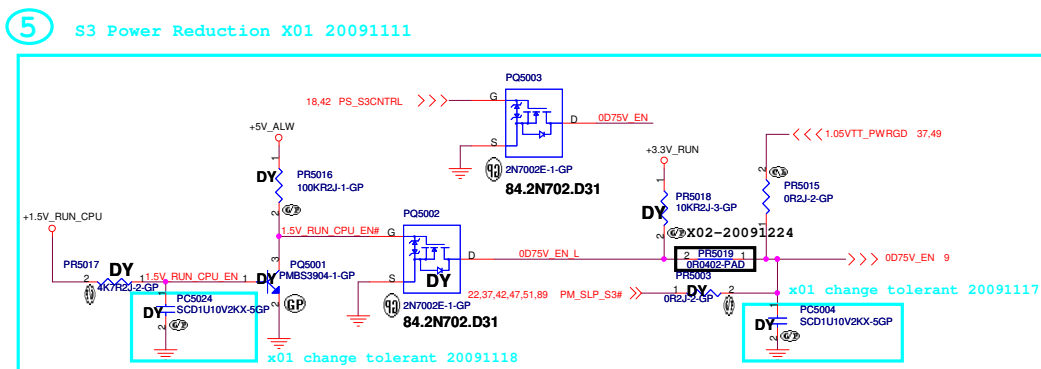
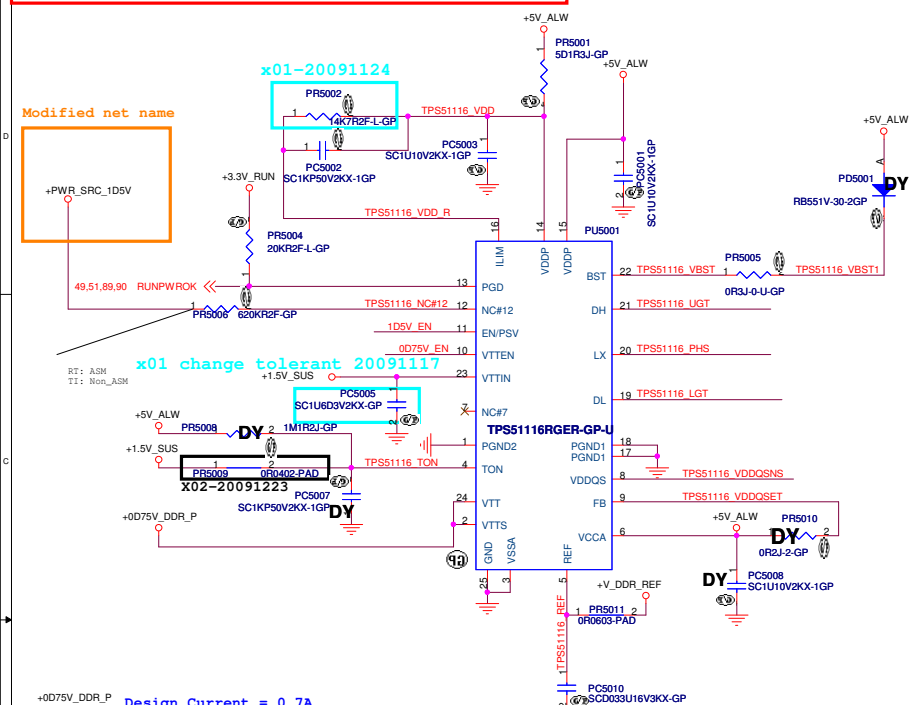
Size	Document Number	Rev
A3	Berry	A00

Date: Wednesday, February 10, 2010	Sheet 48 of 92
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TPS51218 for +1.05V_VTT



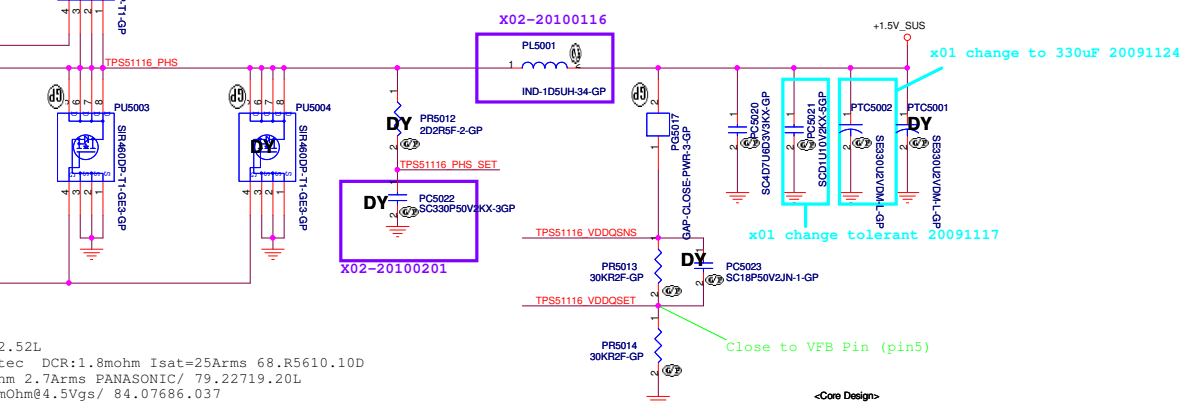
```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V51N	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56mN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 220U 2V EEFXC0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: Si7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz



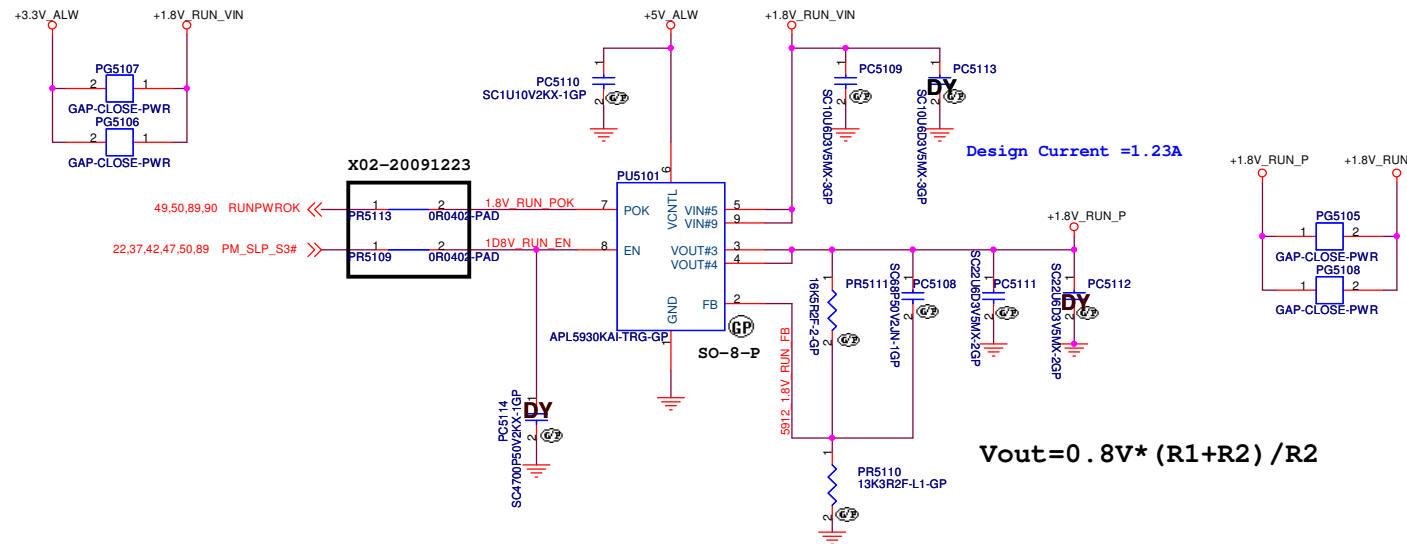
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Title				TPS51116 +1.5V SUS			
Size		Document Number				Rev	
Custom		Berry				A00	
Date: Monday, March 29, 2011				Sheet 50 of 92			

```
SSID = PWR.Plane.Regulator_1p8v
```

APL5930 for +1.8V_RUN


$$V_{out} = 0.8V * (R1 + R2) / R2$$


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Title

APL5930 +1.8V RUN

Size
A3

Document Number
Berry


Rev
A00

Date: Monday, March 29, 2010

Sheet 51 of 92

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Title

Size
A3

Document Number
Berry

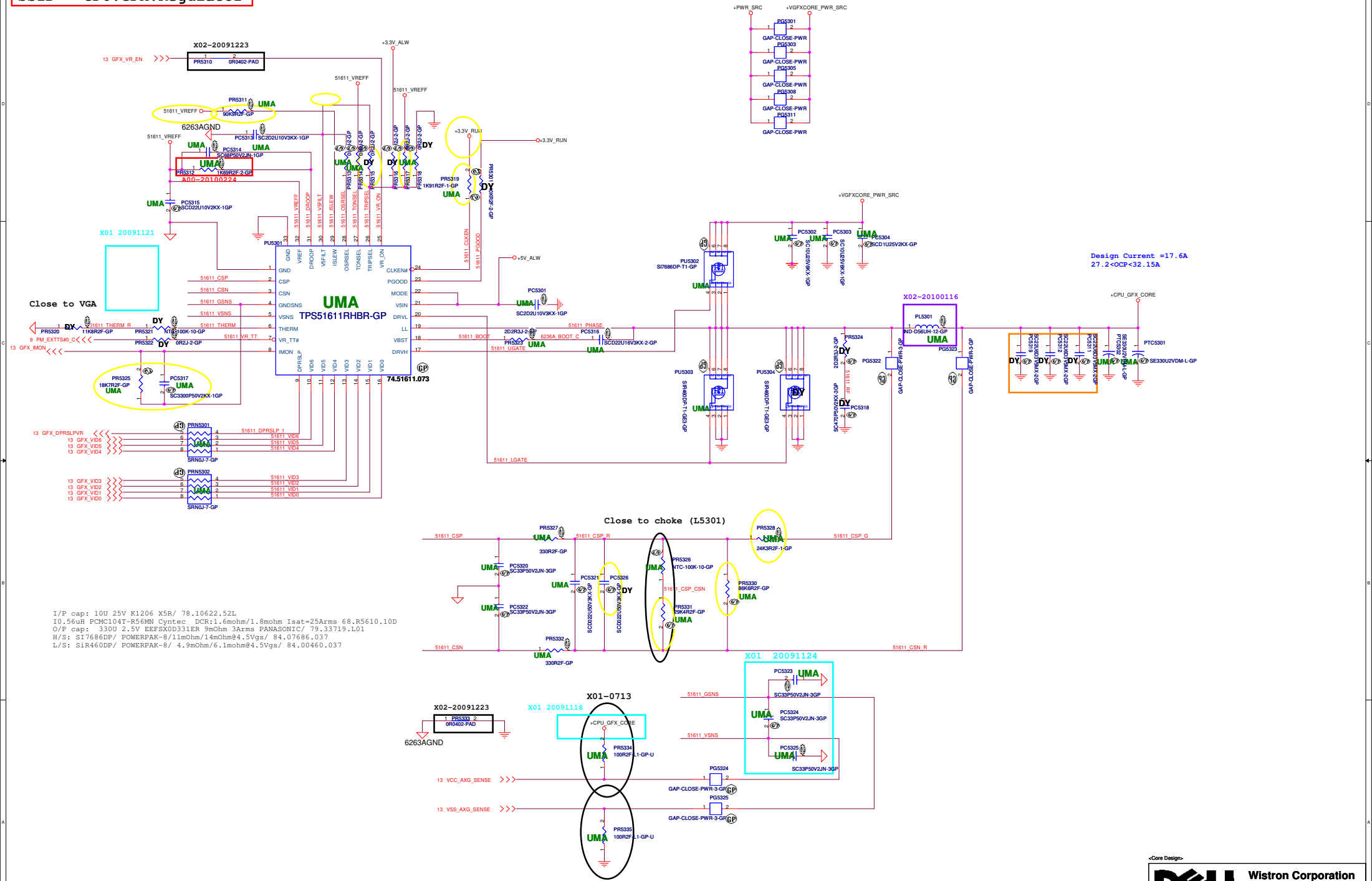
Date: Wednesday, February 10, 2010

Rev
A00

Sheet 52 of 92

Reserved

SSID = CPU.GFX.Regulator



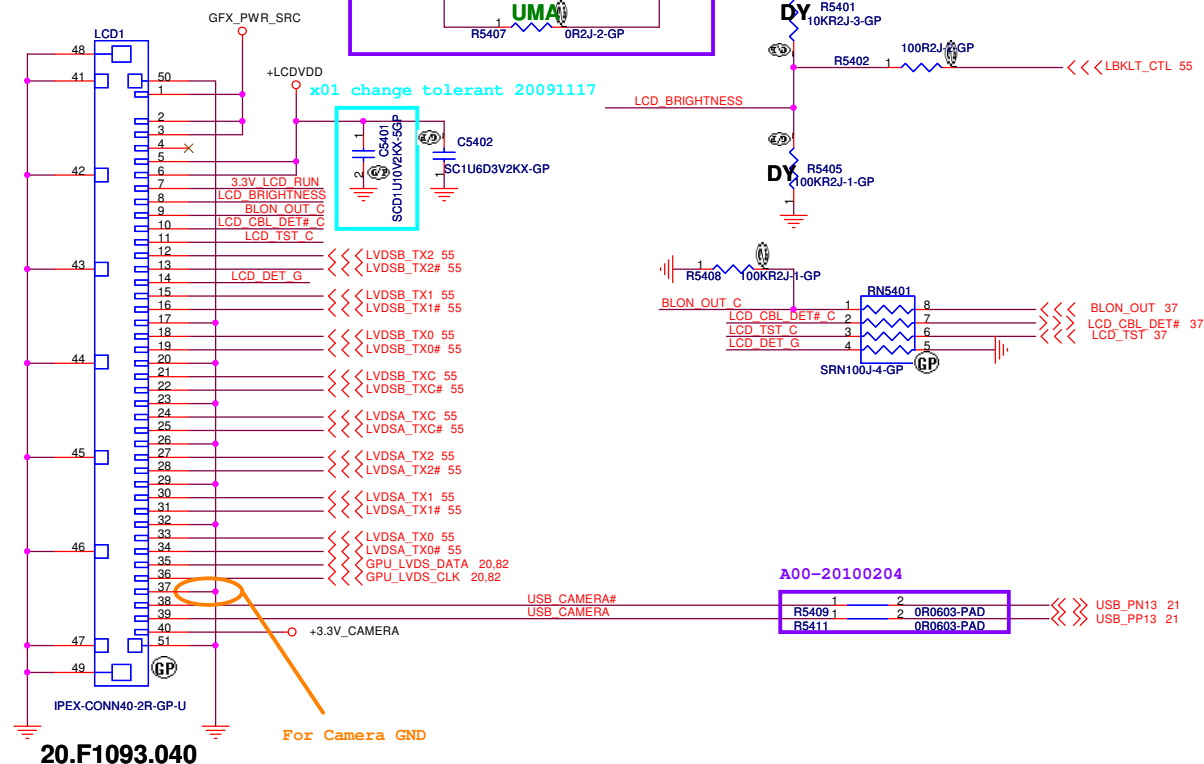
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
10.56uH PCMC104T-R56MN Cynotec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX00331ER 9mOhm 3Arms PANASONIC/ 79.33719.101
H/S: SI7686DP/ POWERPAK-8/11mohm/14mohm@4.5Vgs/ 84.07686.037
L/S: SI7460DP/ POWERPAK-8/ 4.9mohm/6.1mohm@4.5Vgs/ 84.00460.037

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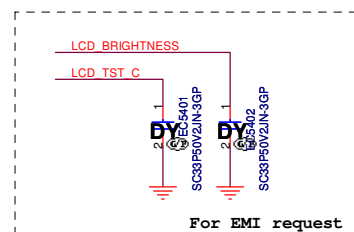
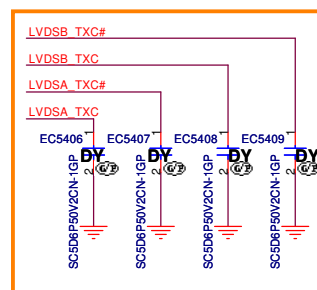
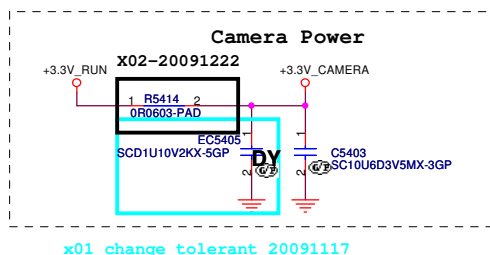
SSID = VIDEO

x02-20091208

LVDS CONNECTOR

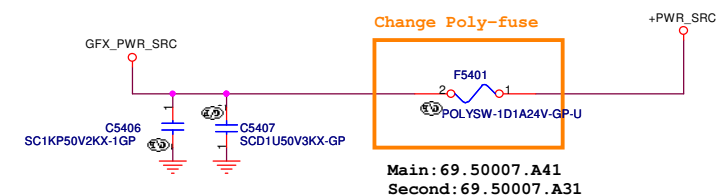


Close to LVDS connector



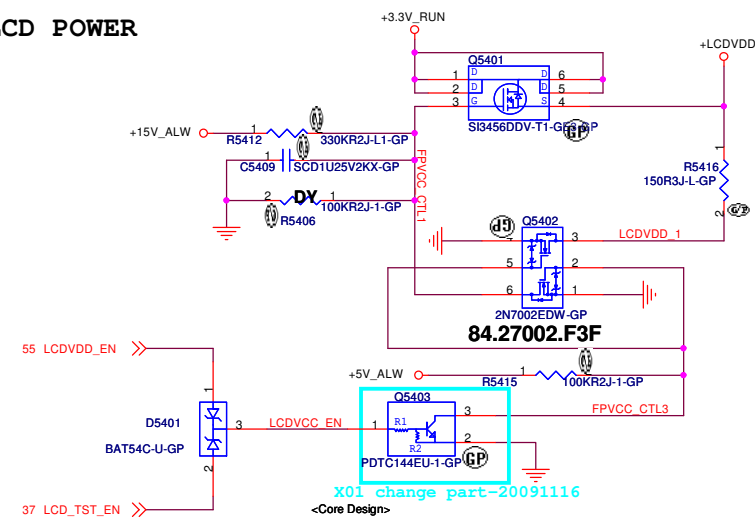
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



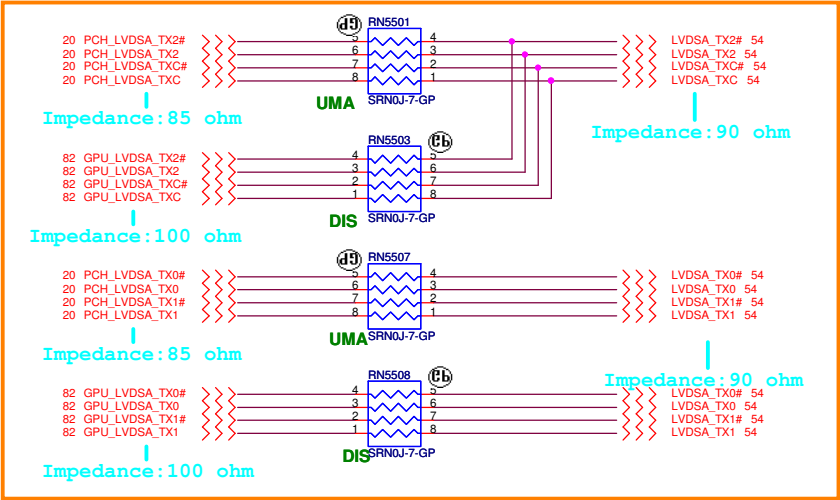
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Title **LCD/Inverter Connector**

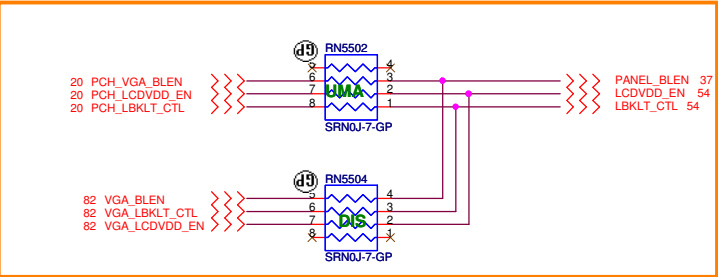
Size A3	Document Number Berry	Rev A00
Date: Monday, March 29, 2010	Sheet 54 of 92	

<http://adefix.vn>

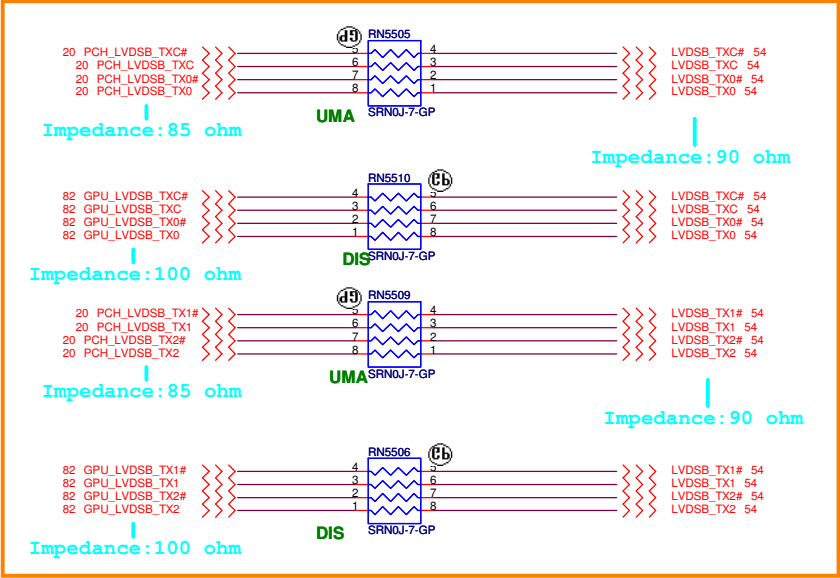
LVDS Channel A



Panel BL brightness/Power En/BL En




LVDS Channel B



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Title

LVDS Switch

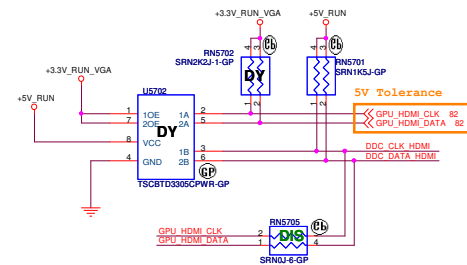
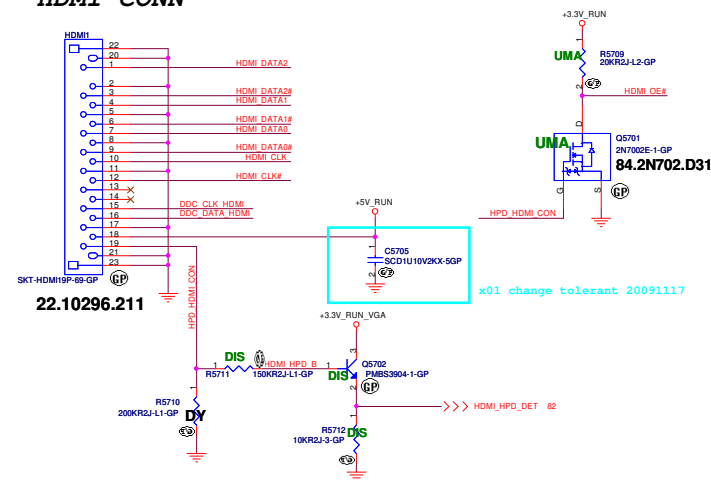
Size
A3

Document Number
Berry

Rev
A00

Date: Wednesday, February 10, 2010Sheet 56 of 92

HDMI CONN

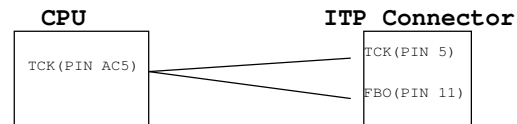


&ltCore Design>

```
SSID = User.Interface
```

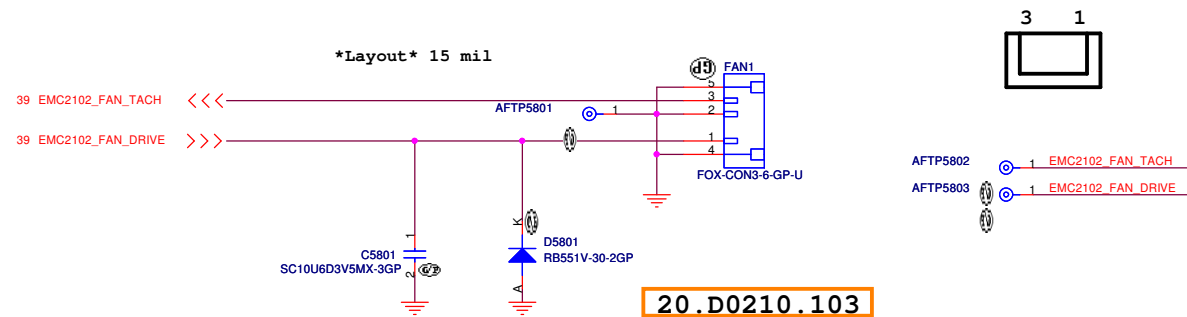
ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



SSID = Thermal

Fan Connector



20.D0210.103

<Core Design>

DELL

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Title	Author	Year	Journal	Volume	Page
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ITP/Fan Connector

Size	A3
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Document Number	Bo...
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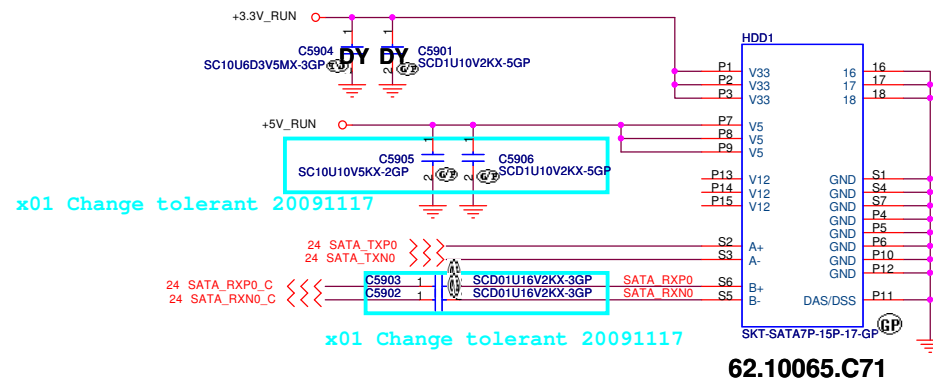
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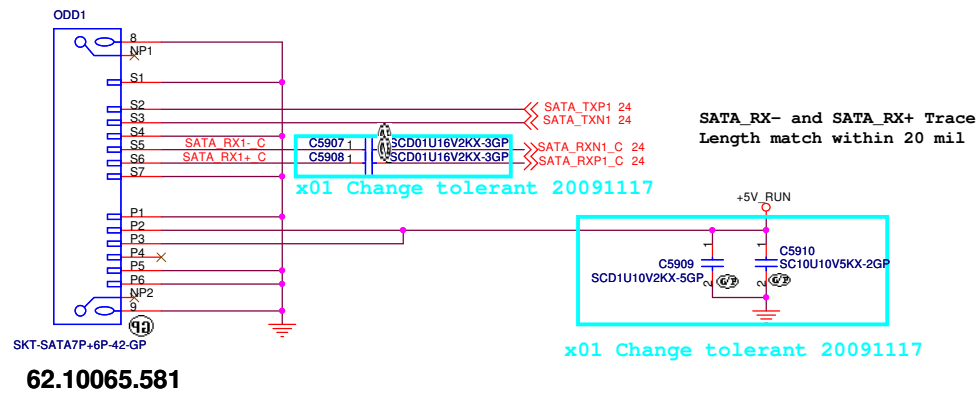
Sheet 58 of 92

SSID = SATA

SATA HDD Connector



ODD Connector



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Title	
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HDD/ODDSize
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BerryRev
400

Date: Monday, March 29, 2010

Sheet 59 of

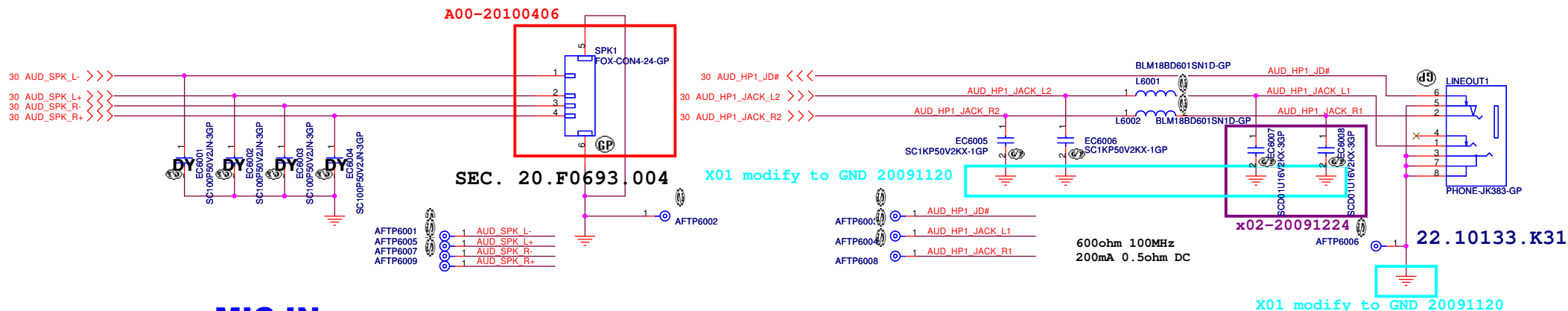
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<http://adl-hy.com>

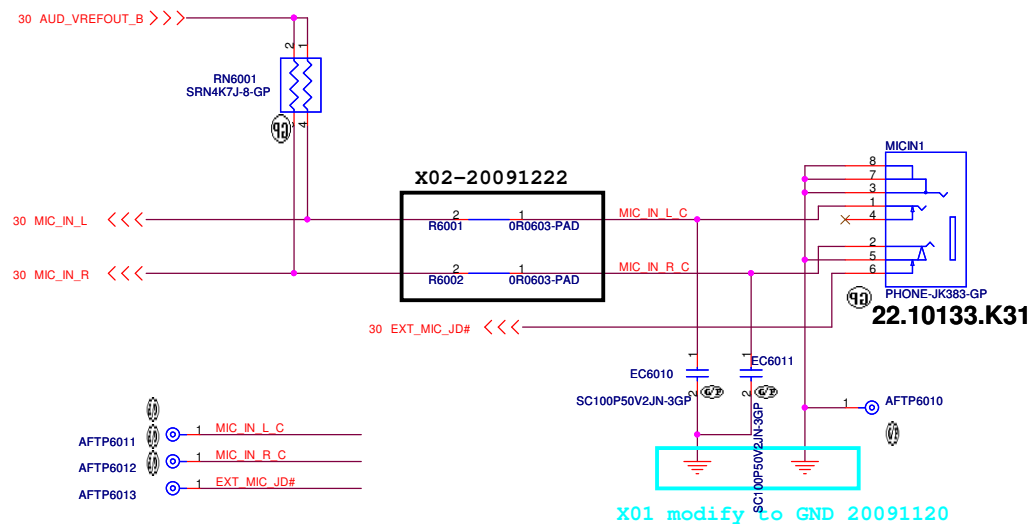
SSID = AUDIO

Speaker Connector

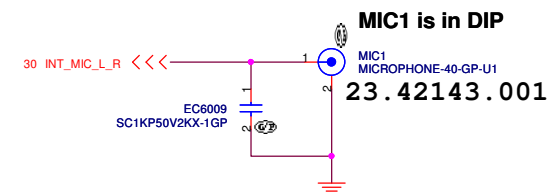
LINE1 OUT



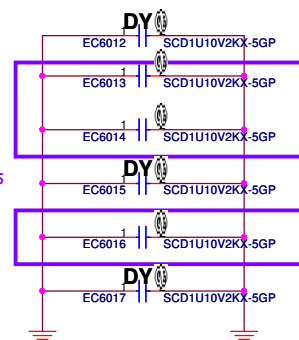
MIC IN



Internal Microphone



X02-20100206



<Core Design>



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Title

Audio Jack

Size

Document Number

Berry

Rev


A00

Date: Monday, April 26, 2010

Sheet 60 of 92

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
Berry

Date: Wednesday, February 10, 2010

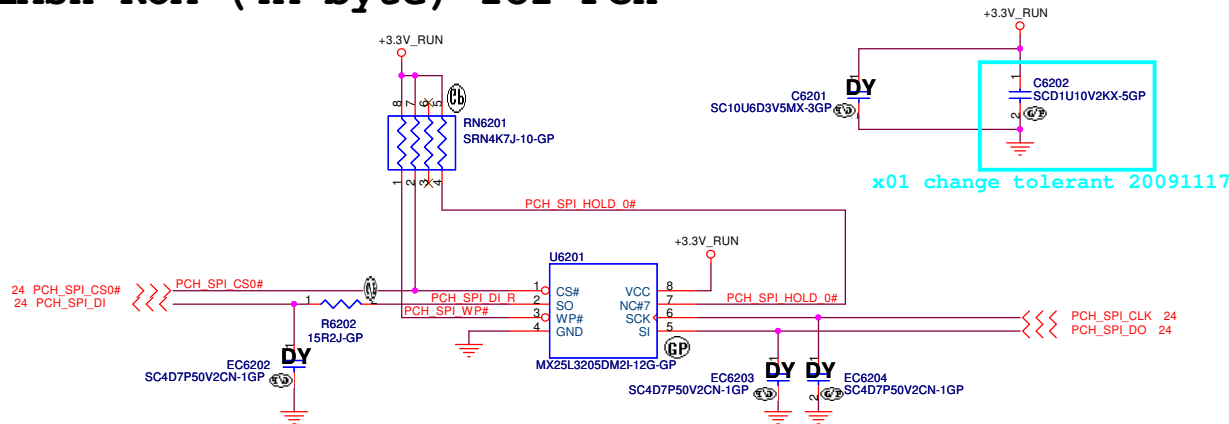
Rev
A00

Sheet 61 of 92

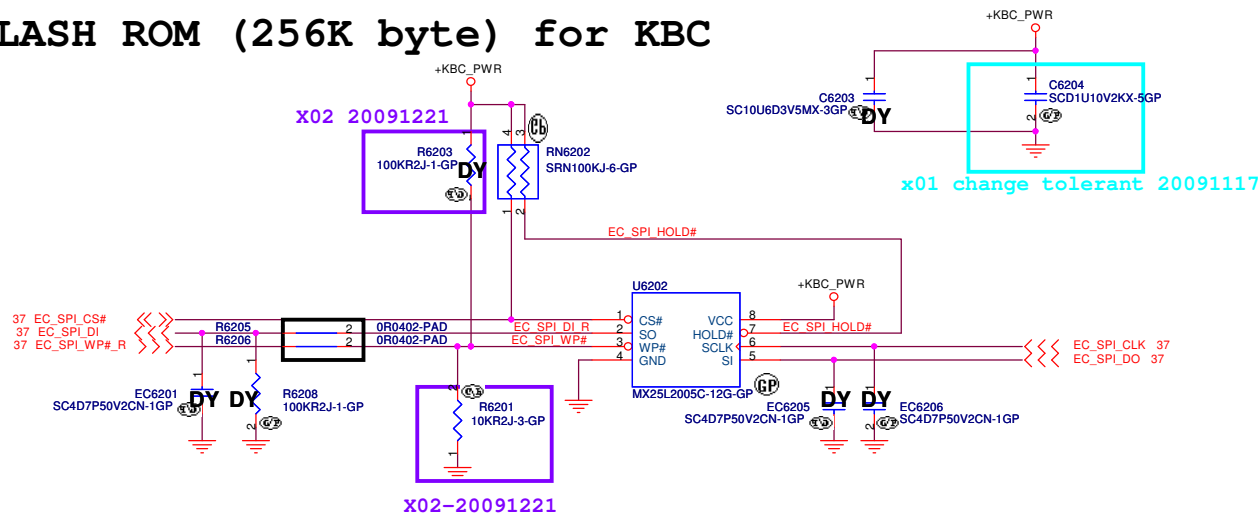
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SSID = Flash.ROM

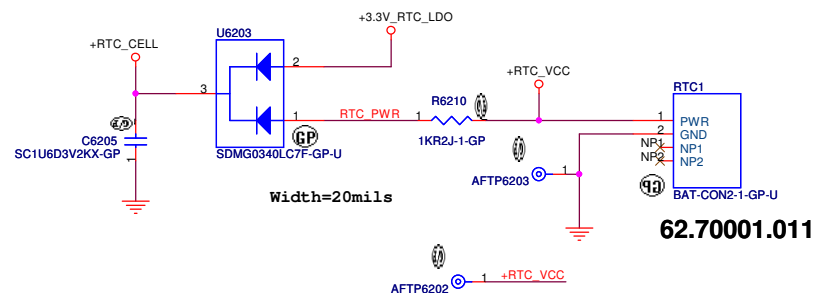
SPI FLASH ROM (4M byte) for PCH



SPI FLASH ROM (256K byte) for KBC



SSID = RBATT



<Core Design>

DELL

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Title

Flash/RTC

Size
A3

	Document Number
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Rev
400

Date: Monday, March 29, 2010

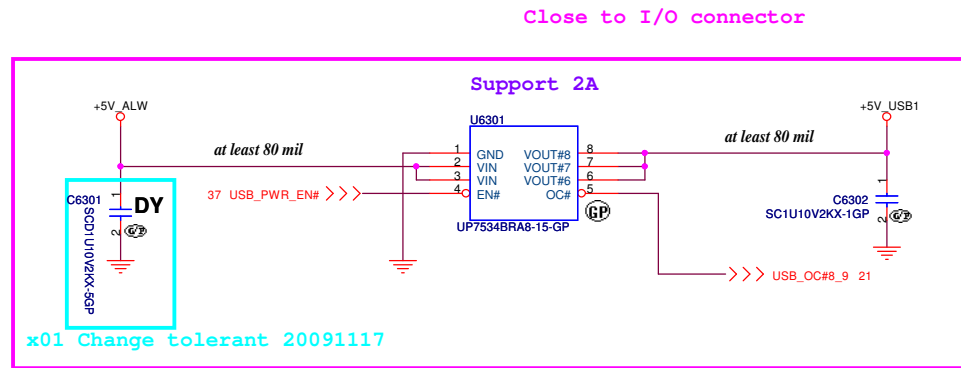
Sheet	62	of	92
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<http://adef.net.vn>

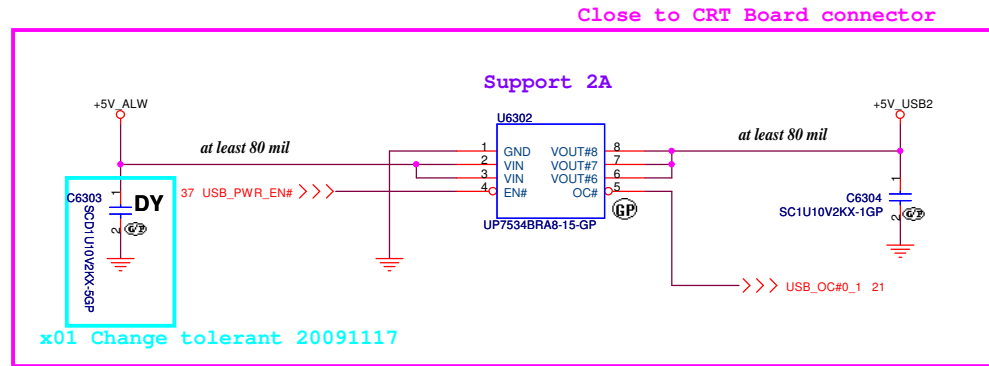
SSID = USB

IO Board USB Power

USB POWER SW
Main UP7534BRA8-15 P/N:74.07534.079
SEC AP2101MPG-13 P/N: 74.02101.079



CRT Board USB Power



<Core Design>



Title			Rev
USB Power SW			A00
Size	Document Number	Berry	
Date: Monday, March 29, 2010	Sheet 63	of	92

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<Core Design>



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Title

Reserved

Size
A4

Document Number
Berry


Rev
A00

Date: Wednesday, February 10, 2010

Sheet 64 of 92

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
Berry

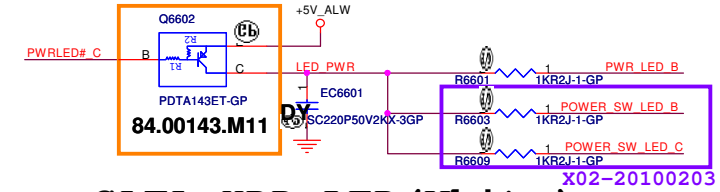
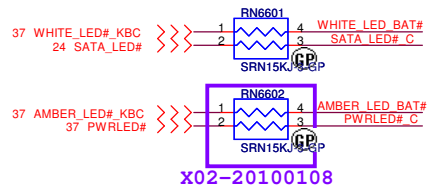
Date: Wednesday, February 10, 2010

Rev
A00

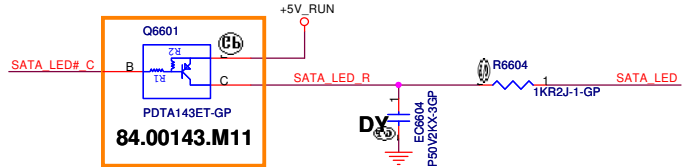
Sheet 65 of 92

Reserved

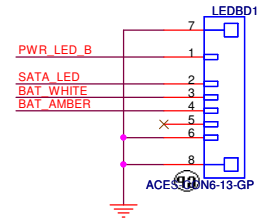
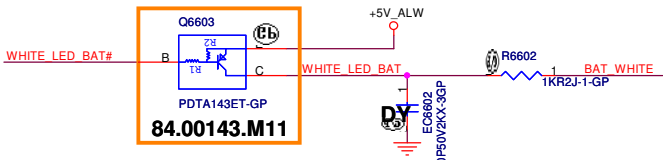
Power LED (White)



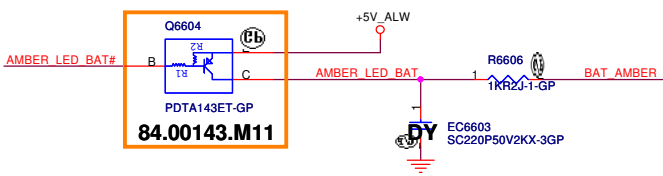
SATA HDD LED (White)



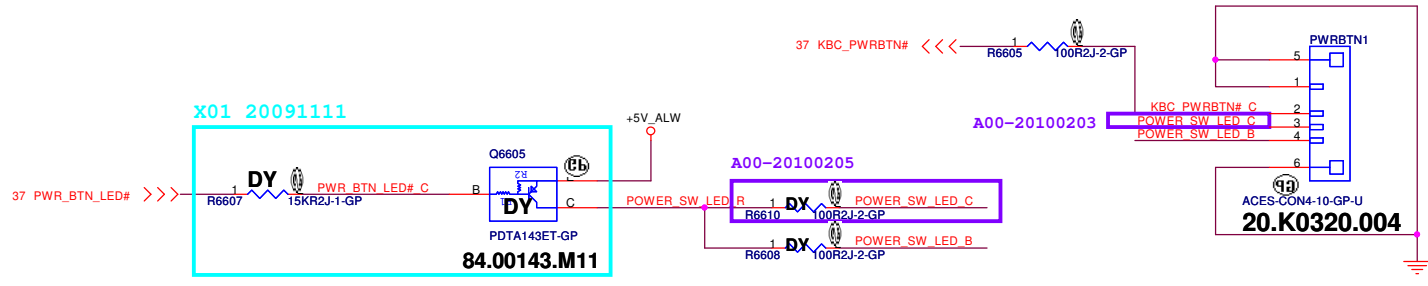
Battery LED1 (White)



Battery LED2 (Amber)




Power button LED (White)



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Title

Size
A3

Document Number
Berry

Date: Wednesday, February 10, 2010

Rev
A00

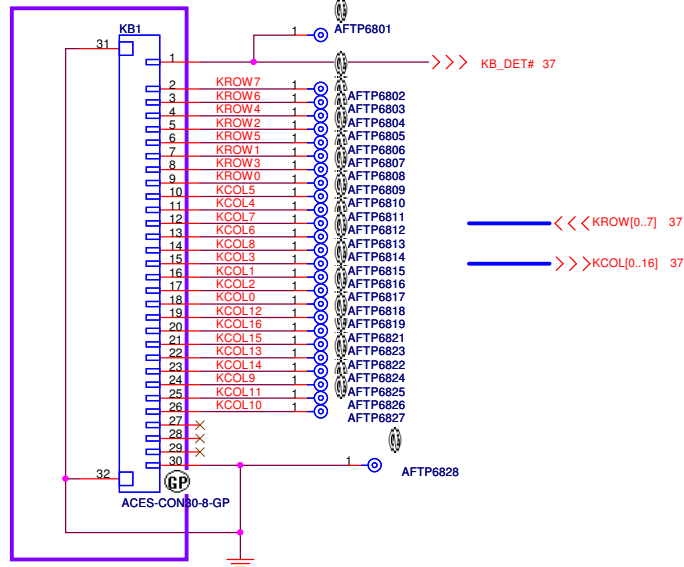
Sheet 67 of 92

Reserved

SSID = KBC

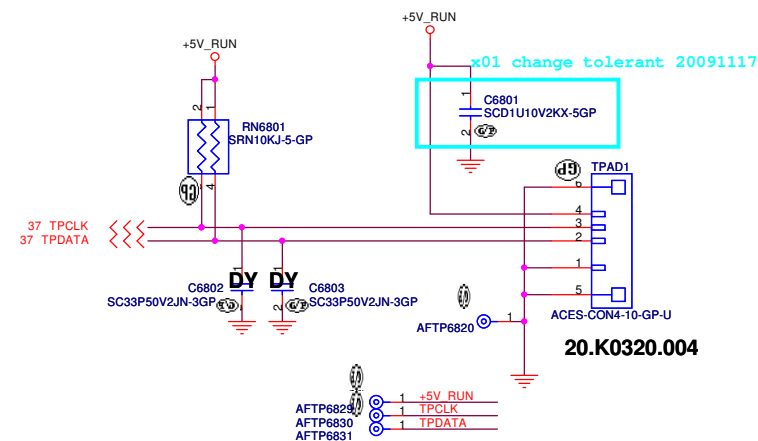
Internal Keyboard Connector

A00-20100203



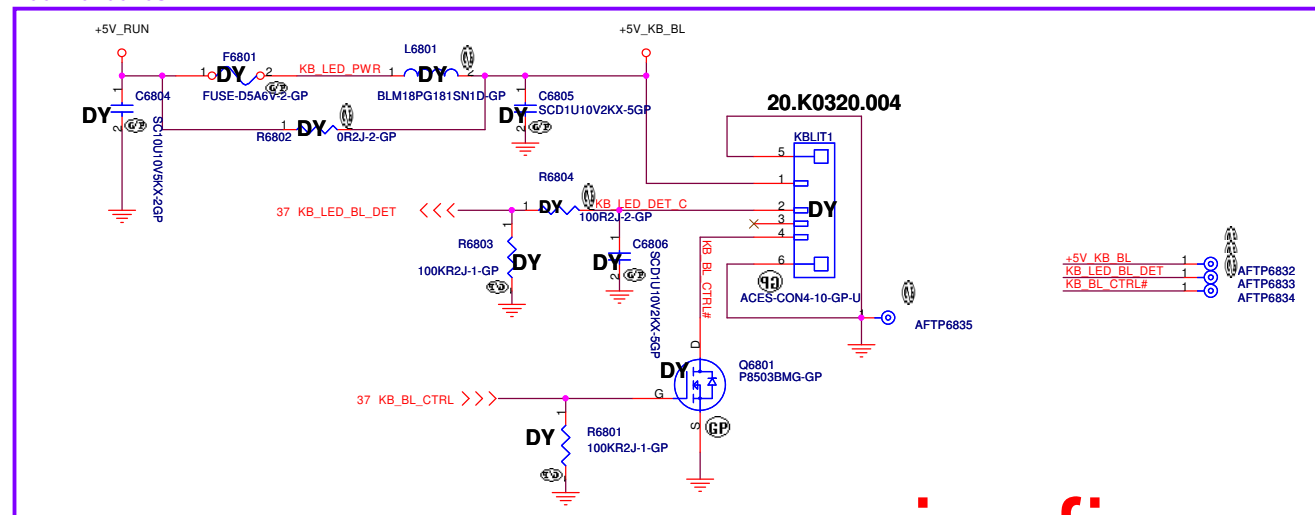
SSID = Touch.Pad

TouchPad Connector



KB Backlight Connector

A00-20100205



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Title

Key Board/Touch Pad

Size

Document Number

Rev

A3

Berry

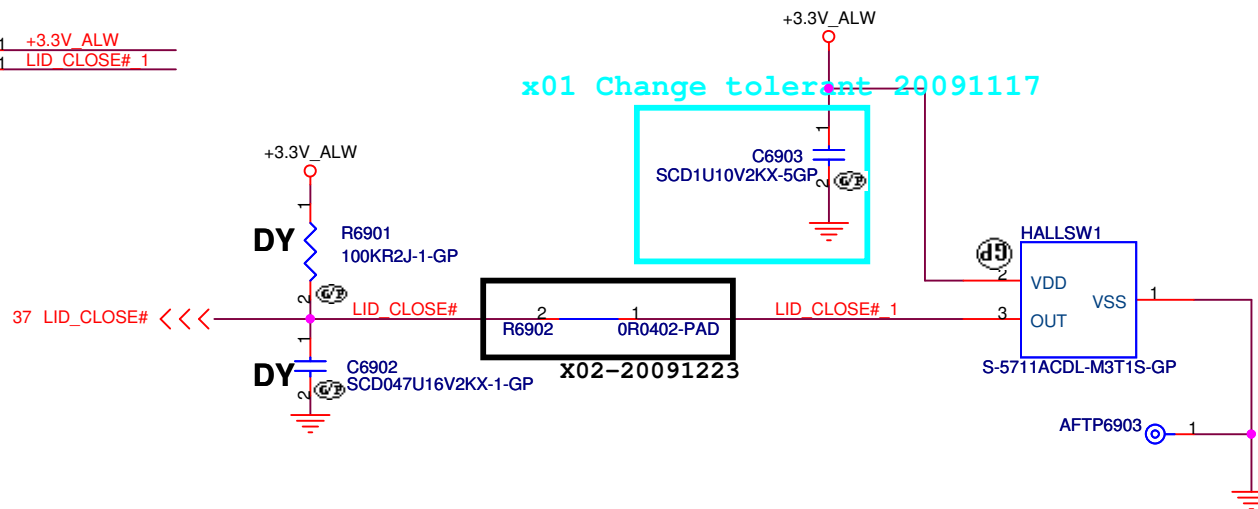
A00

Date: Monday, March 29, 2010

Sheet 68 of 92

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AFTP6901 1 +3.3V_ALW
AFTP6902 1 LID_CLOSE# 1



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Title

Hall Sensor

Size
A4

Document Number

Berry

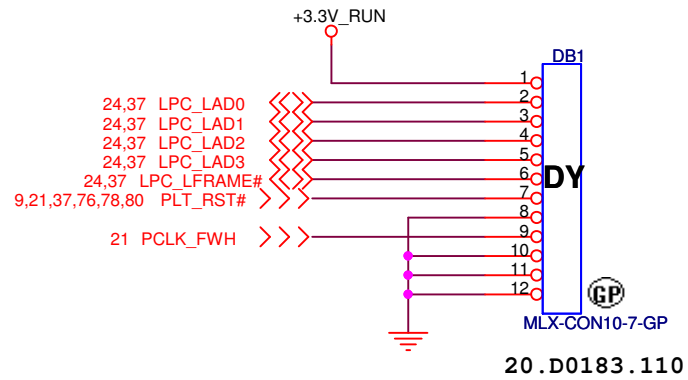
Rev

A00

Date: Monday, March 29, 2010

Sheet 69 of 92

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Title

Dubug connector

Size
A4

Document Number

Berry

Rev
A00


Date: Monday, March 29, 2010

Sheet 70 of 92

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<Core Design>

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Title			
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Size A4	Document Number Berry		Rev A00
Date: Wednesday, February 10, 2010		Sheet 71 of	92

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

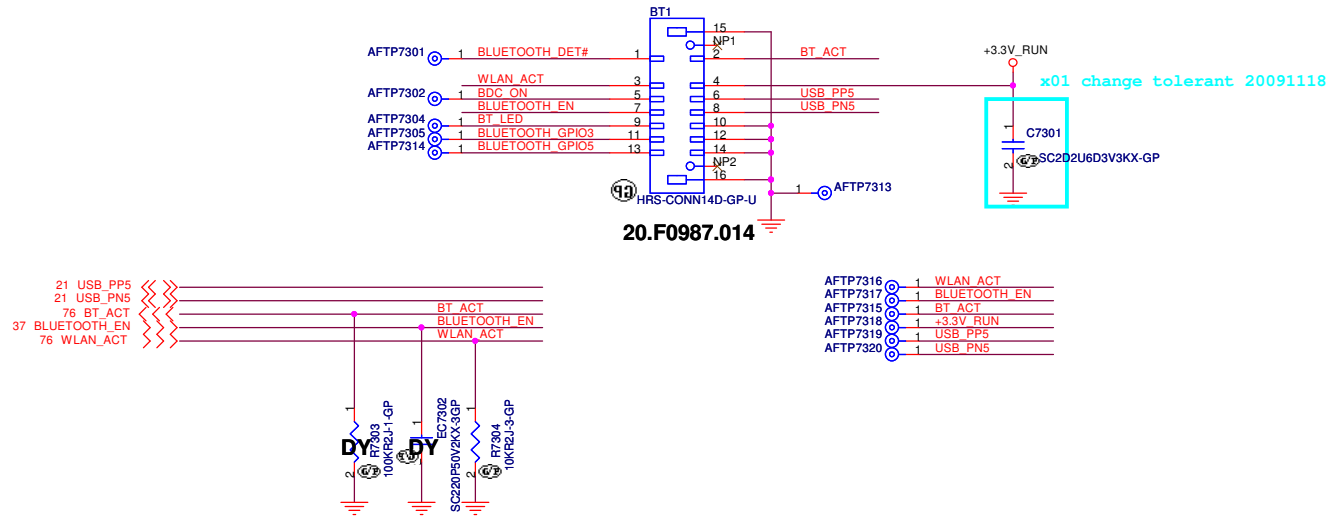
RESERVED

Size A3	Document Number Berry	Rev A00
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Date: Wednesday, February 10, 2010	Sheet 72 of 92
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SSID = User.Interface

Bluetooth Module conn.




<Core Design>

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Title Bluetooth			
Size A3	Document Number Berry	Rev A00	
Date: Monday, March 29, 2010		Sheet 73 of 92	

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.


Title

Reserved

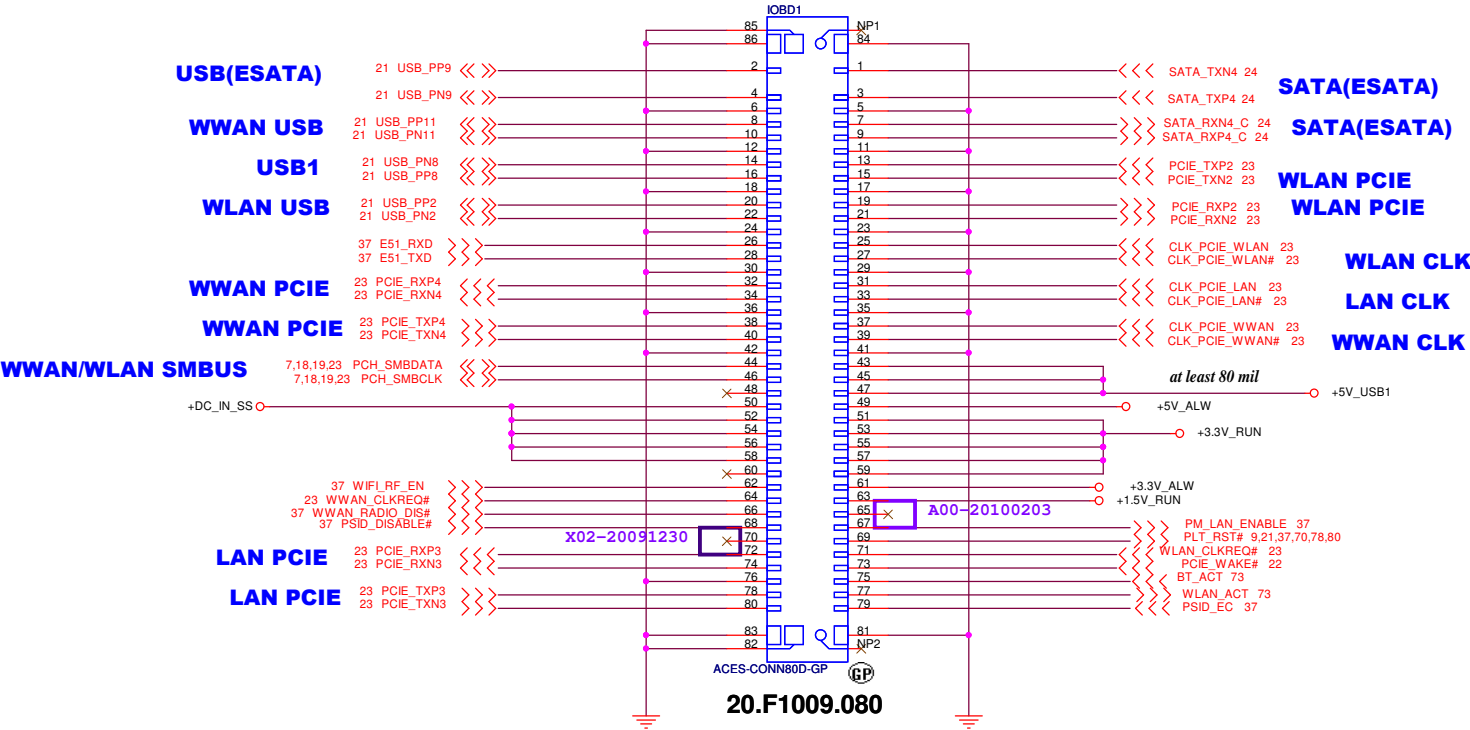
Size A3	Document Number Berry	Rev A00
Date: Wednesday, February 10, 2010	Sheet 74 of 92	

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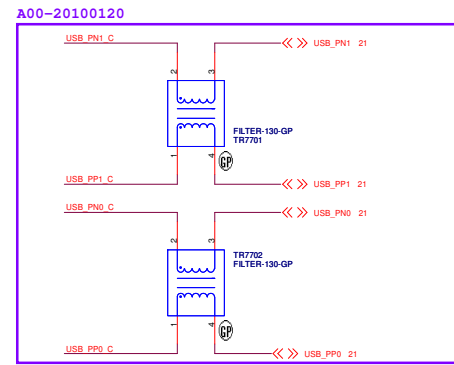
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number Berry		Rev A00
Date: Wednesday, February 10, 2010		Sheet 75 of	92

IO Board CONN 80 pin



Pinout diagram for the ACES-CON20-1-GP-U connector. The diagram shows a 20-pin connector with pins numbered 1 to 20. Pin 1 is labeled 'at least 80 mil'. Pin 2 is labeled '+5V_USB2'. Pin 3 is labeled 'USB PNT C'. Pin 4 is labeled '+5V_RUN'. Pin 5 is labeled 'USB PPT C'. Pin 6 is labeled 'USB PNO C'. Pin 7 is labeled 'USB PPO C'. Pin 8 is labeled 'CRT R'. Pin 9 is labeled 'CRT G'. Pin 10 is labeled 'CRT B'. Pin 11 is labeled 'CRT H/VSYNC'. Pin 12 is labeled 'CRT VSYNC CON'. Pin 13 is labeled 'CRT DDCLK CON'. Pin 14 is labeled 'CRT DDCLKA CON'. Pin 15 is labeled 'CRT DDCLKB CON'. Pin 16 is labeled 'CRT DDCLKC CON'. Pin 17 is labeled 'CRT DDCLKD CON'. Pin 18 is labeled 'CRT DDCLK E CON'. Pin 19 is labeled 'CRT DDCLK F CON'. Pin 20 is labeled 'CRT DDCLK G CON'. The connector is labeled 'ACES-CON20-1-GP-U' and '20.F0772.020'. The diagram also shows a ground symbol and a label 'SEC. 20.F1035.020'.



Close to CRT Board CONN

Filter design on CRT Board

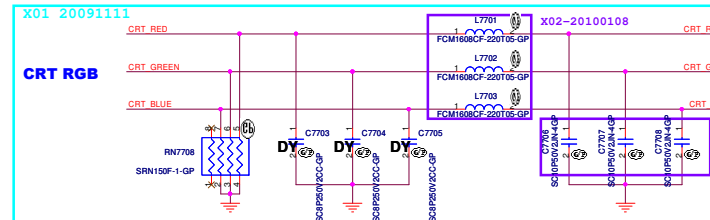
82 VGA_CRT_RED
82 VGA_CRT_GREEN
82 VGA_CRT_BLUE

20 PCH_CRT_RED
20 PCH_CRT_GREEN
20 PCH_CRT_BLUE

BN701
DIS
SPR1U-7-G

BN702
UMA
SPR1U-7-G

CRT_RED
CRT_GREEN
CRT_BLUE

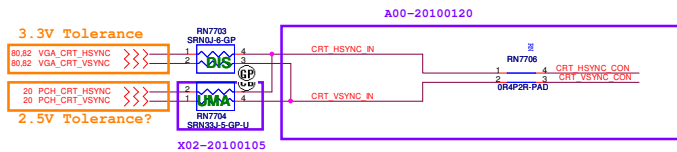


82 VGA_CRT_DDCDATA
82 VGA_CRT_DDCCLK

2 1 4

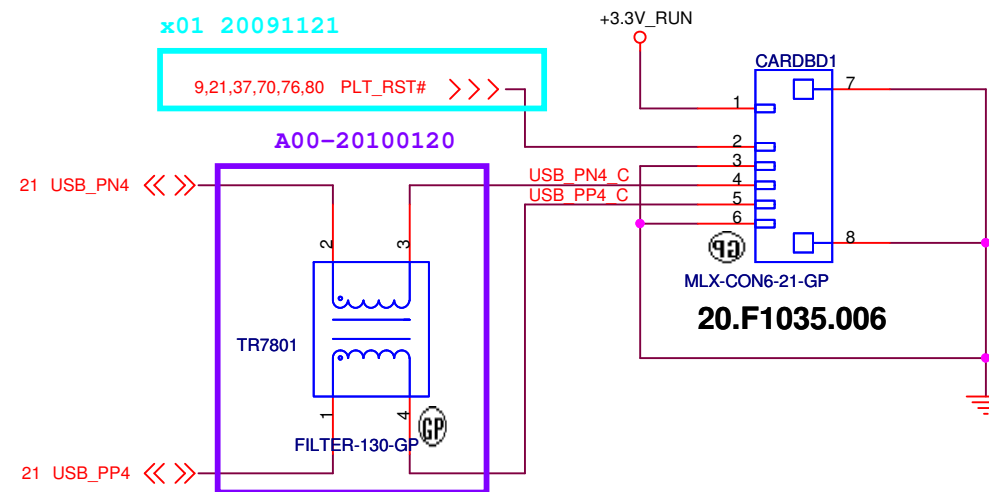
SR90J-6-GP

Crt DDCCLK CON



SSID = SDIO

Card Reader connector



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Title

CARD Reader CONN

Size
A4

Document Number

Berry

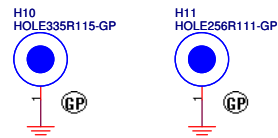
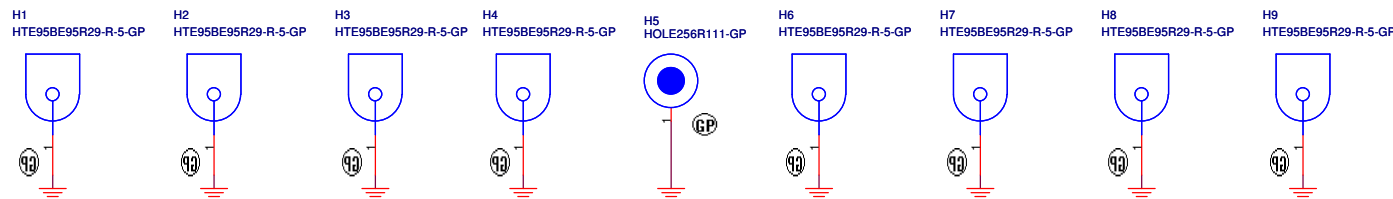
Rev

A00

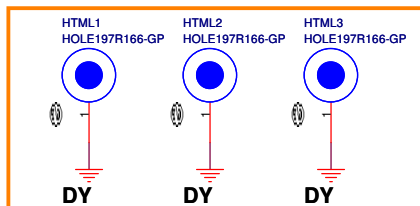
Date: Monday, March 29, 2010

Sheet	78	of	92
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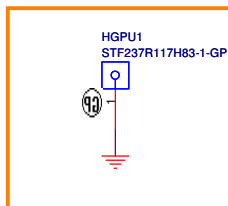
92



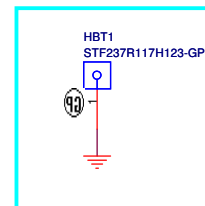
CPU Thermal module hole



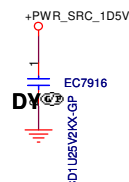
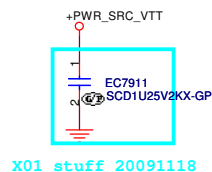
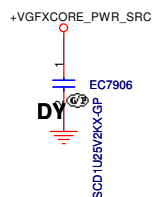
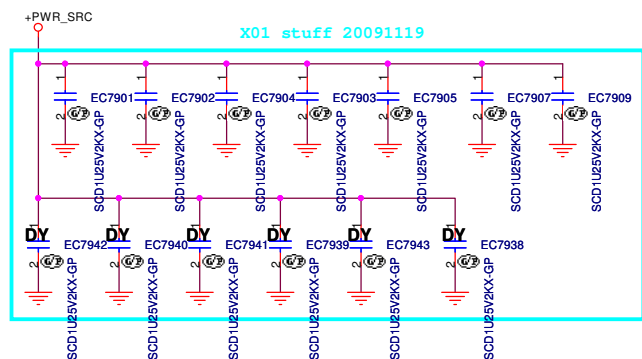
GPU Thermal module hole



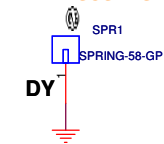
stand off



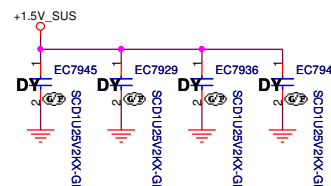
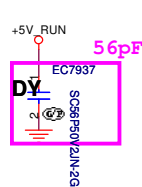
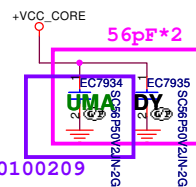
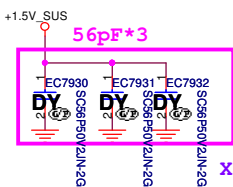
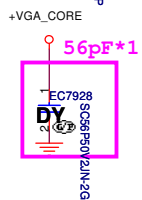
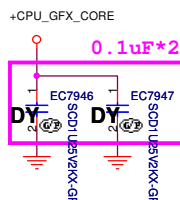
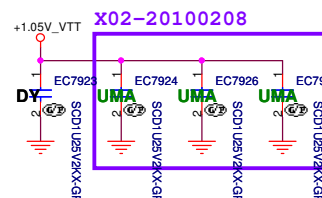
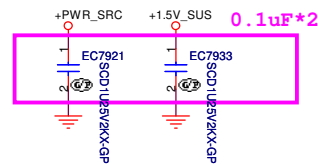
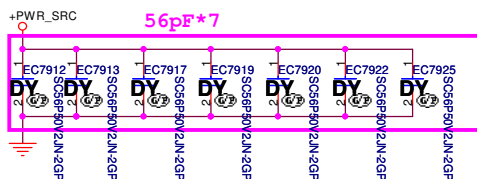
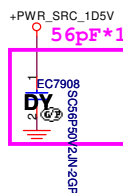
EMI Reserve



EMI Reserve



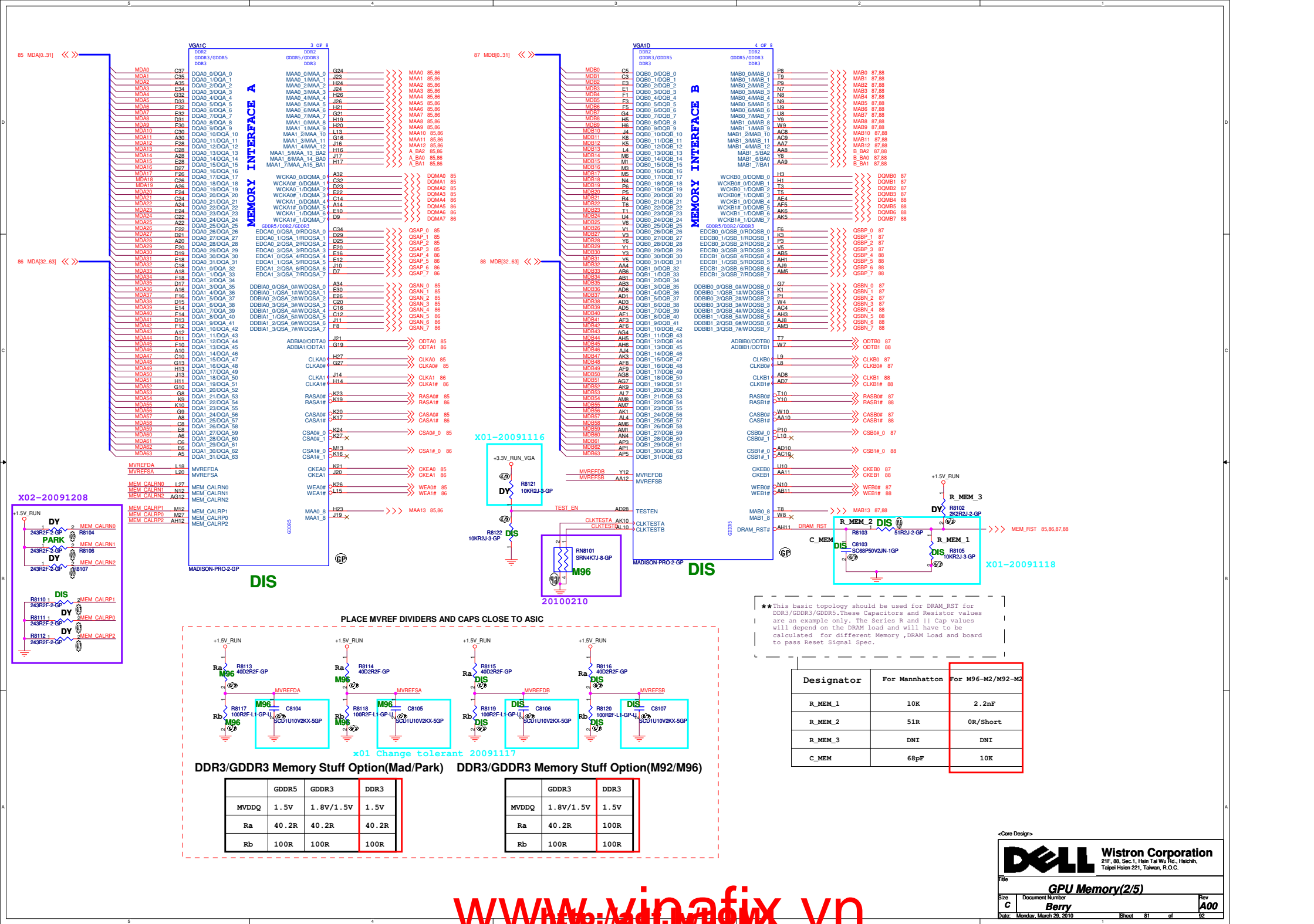
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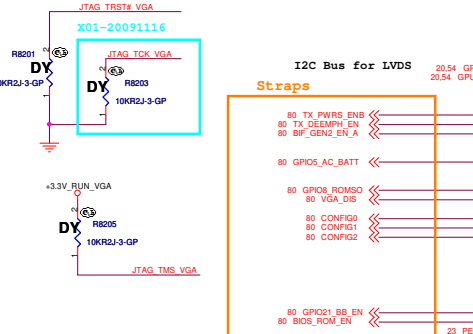
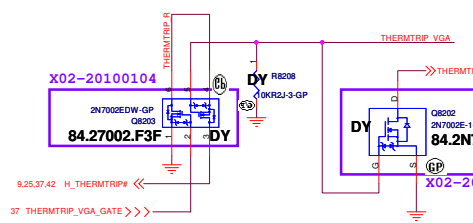
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DELL Wistron Corporation
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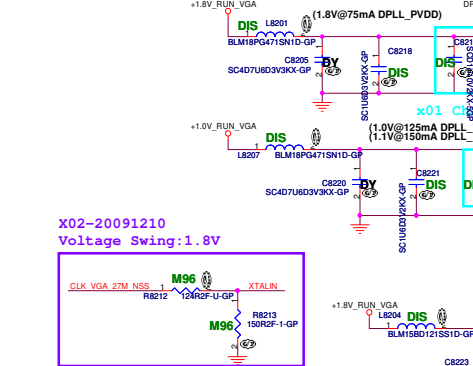
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Size	Document Number	Rev	A00
A3	Berry		
Date:	Wednesday, February 10, 2010	Sheet	79 of 92



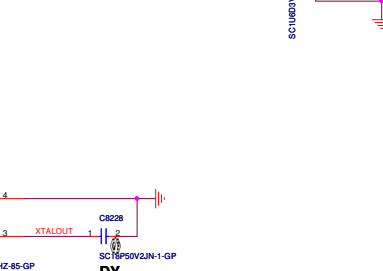
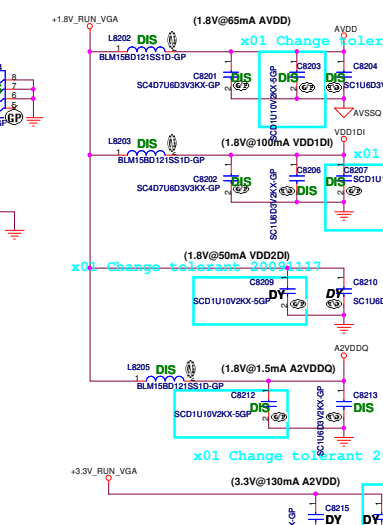
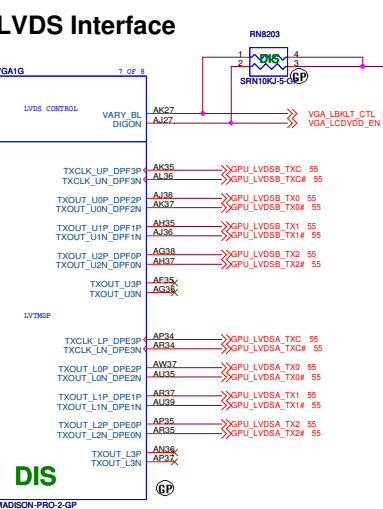
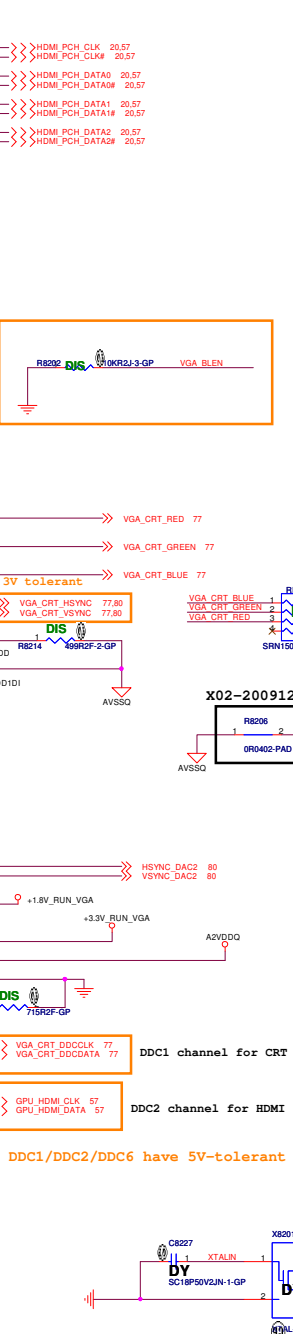
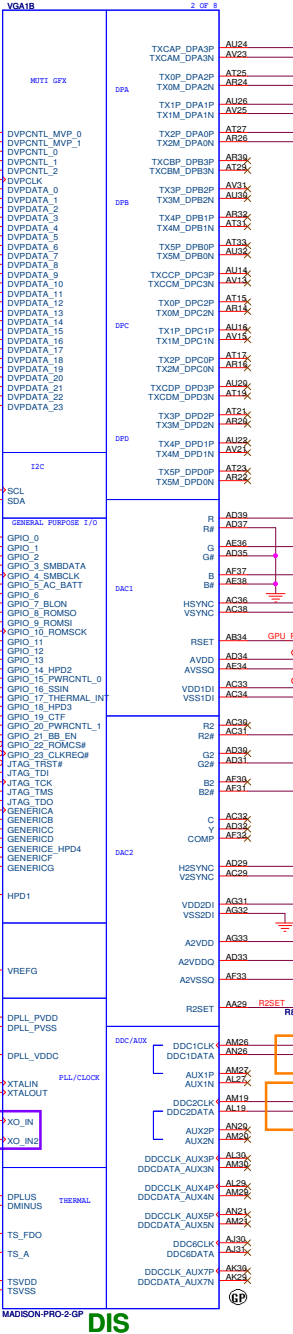
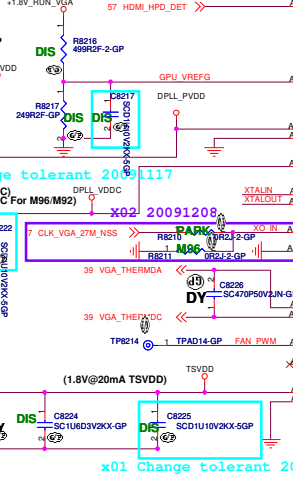
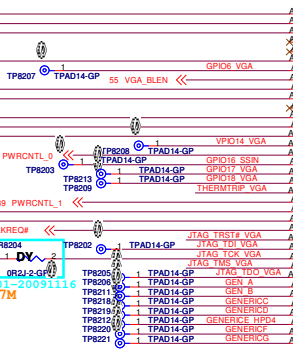
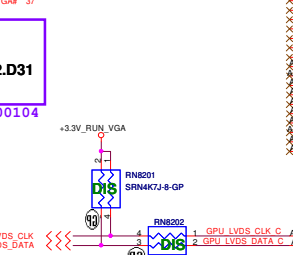
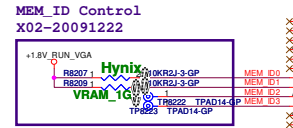
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0001	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz) 64M*16
0011	DDR3 Hynix-H5TQ2G63BFR-12C (800MHz) 128M*16
0010	DDR3 SAMSUNG K4W2G1646B-HC12 (800MHz) 128M*16
0000	DDR3 SAMSUNG-K4W1G1646E-HC12 (800MHz) 64M*16



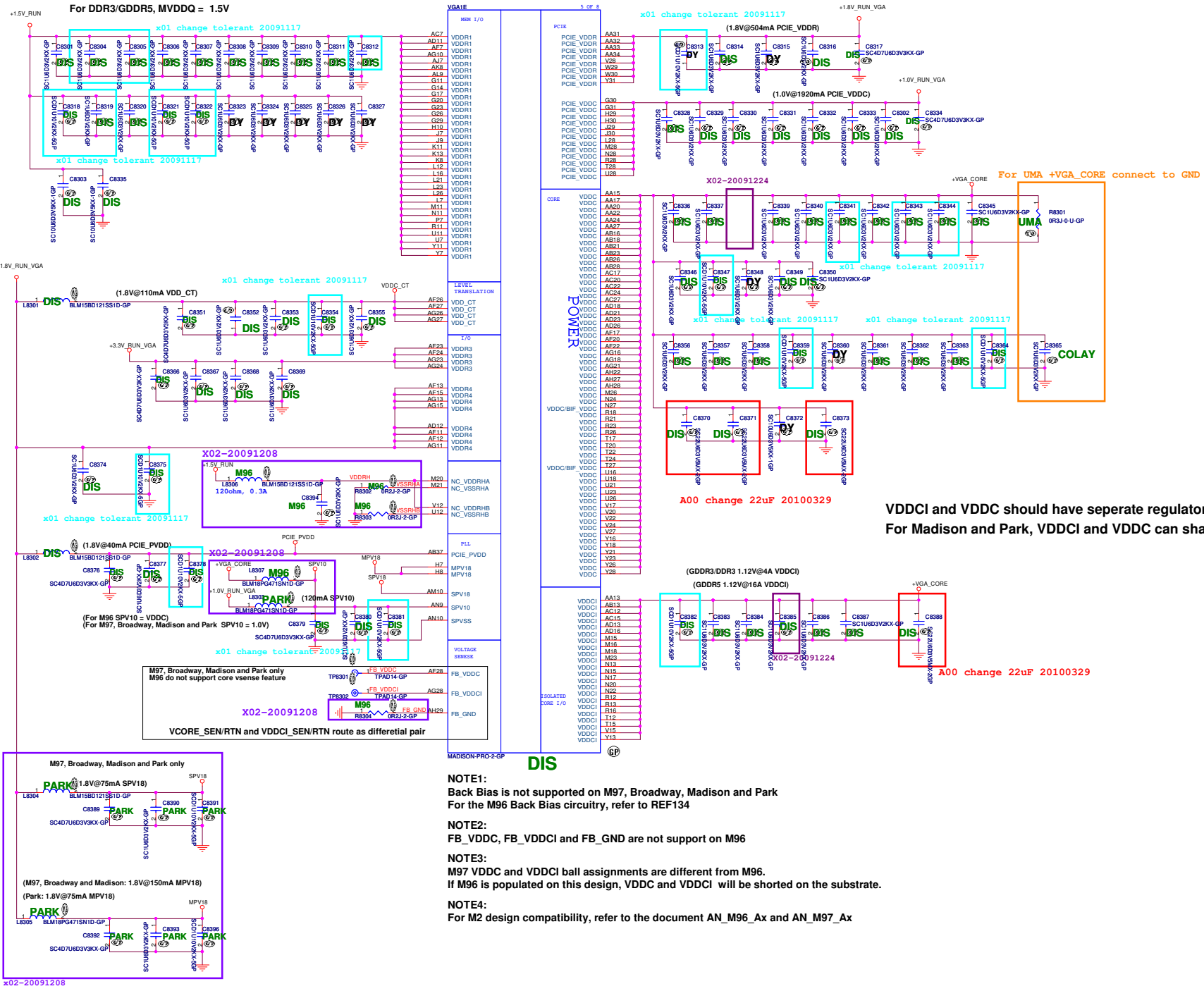
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TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
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JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC



Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO IN (Park, Madison, and Broadway only)

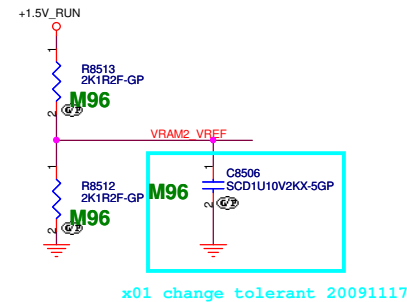
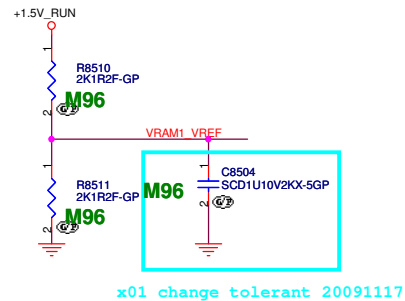
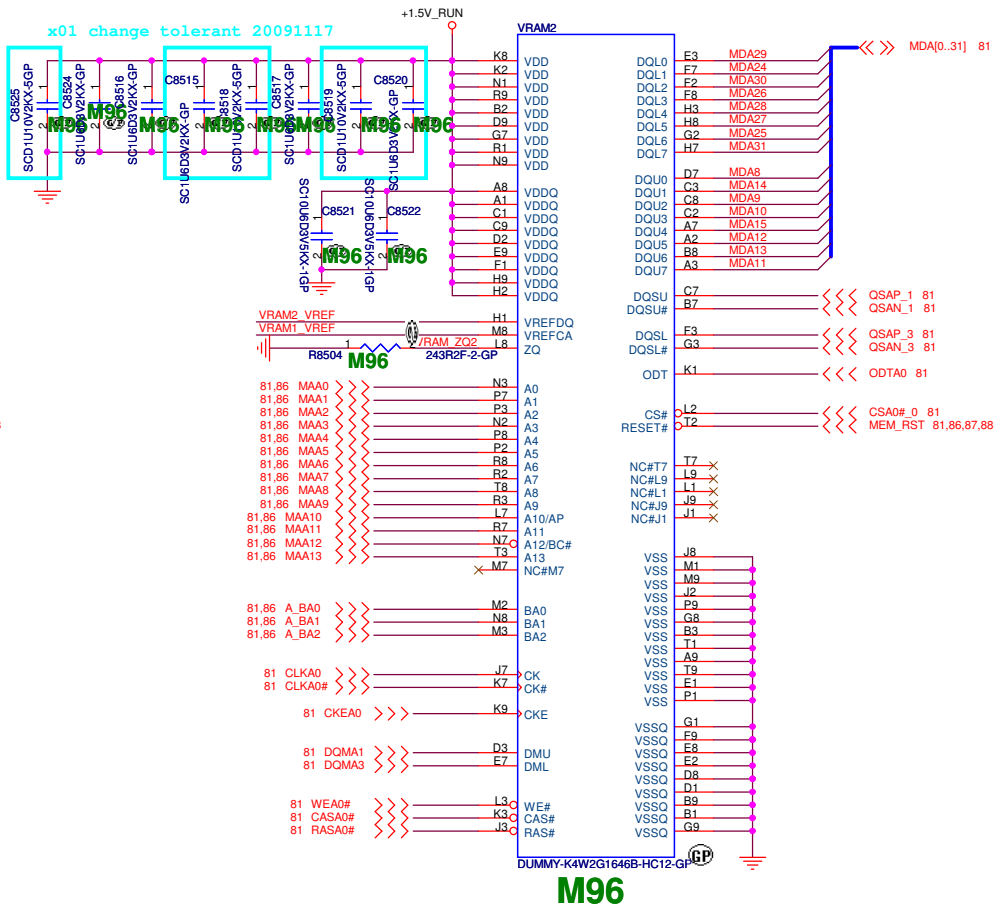
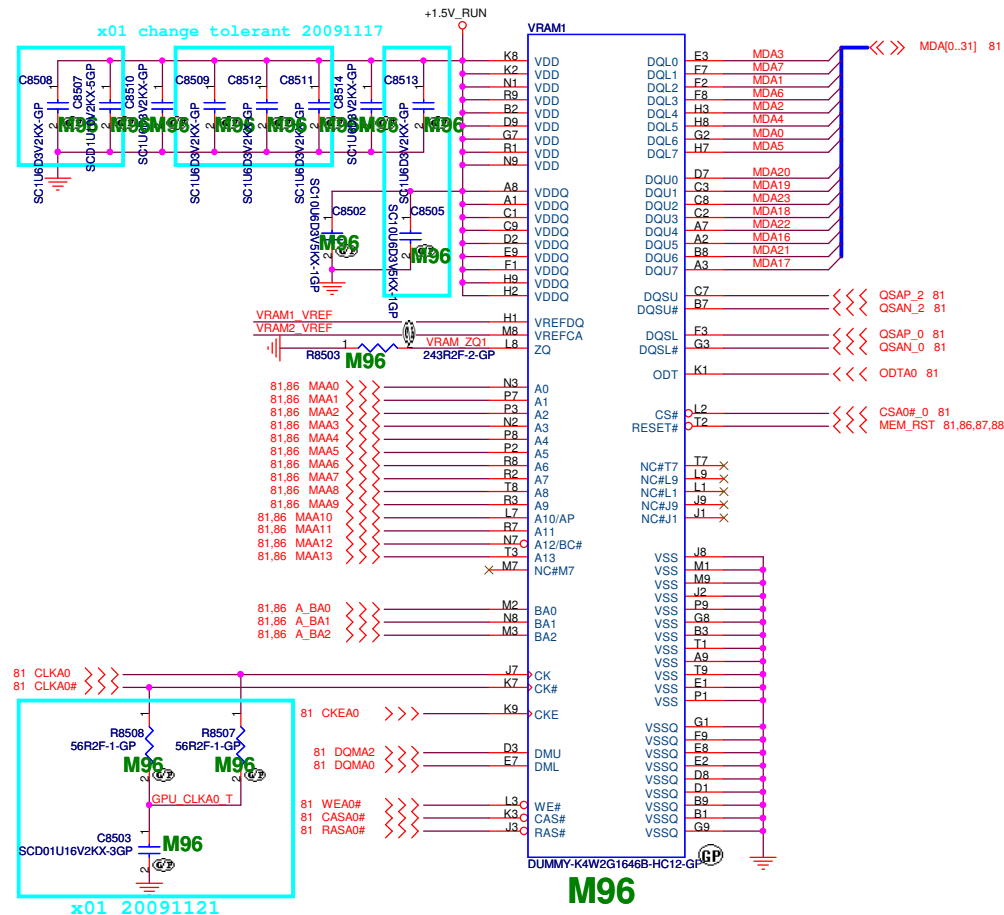


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A2	Berry			A00
Date:	Monday, January 29, 2012	Elapsed	52s	of 53



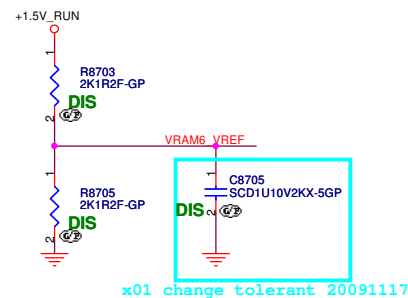
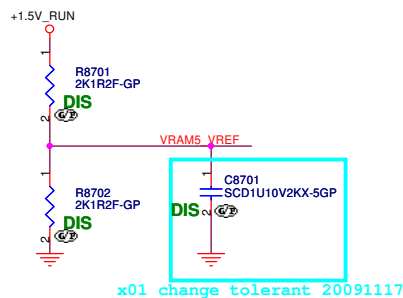
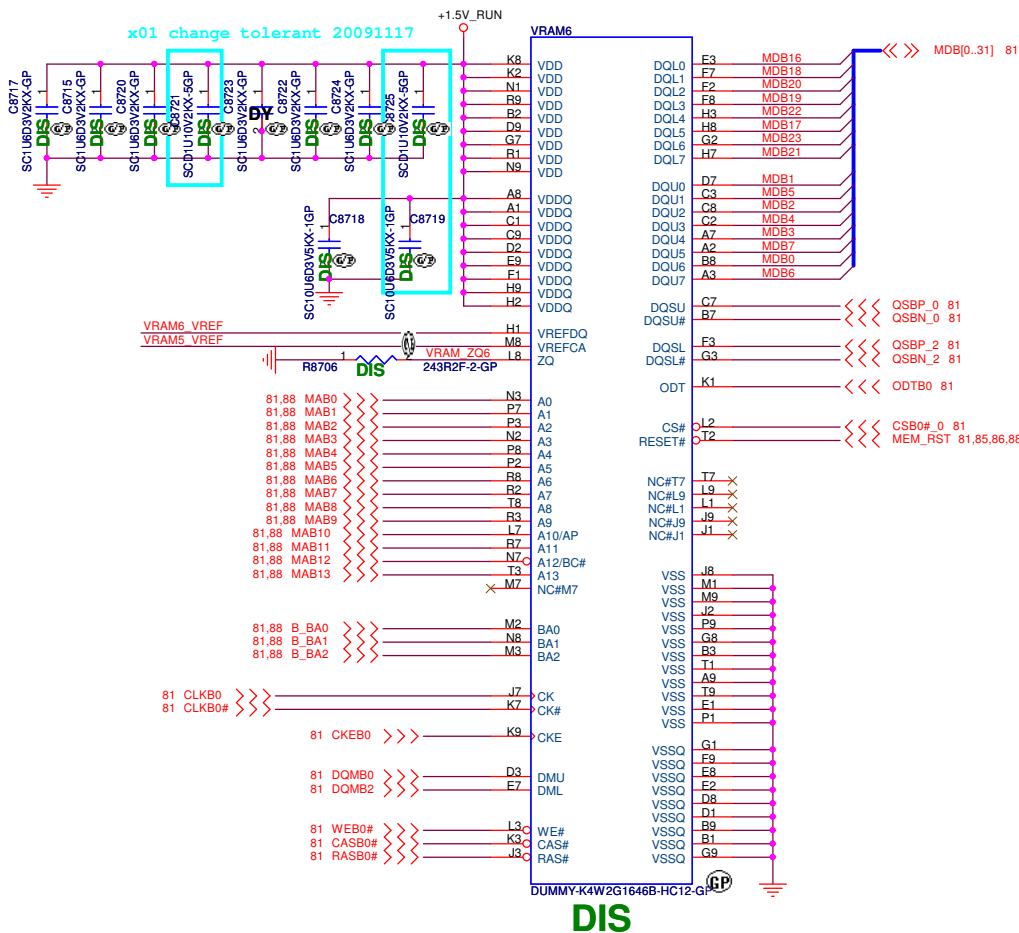
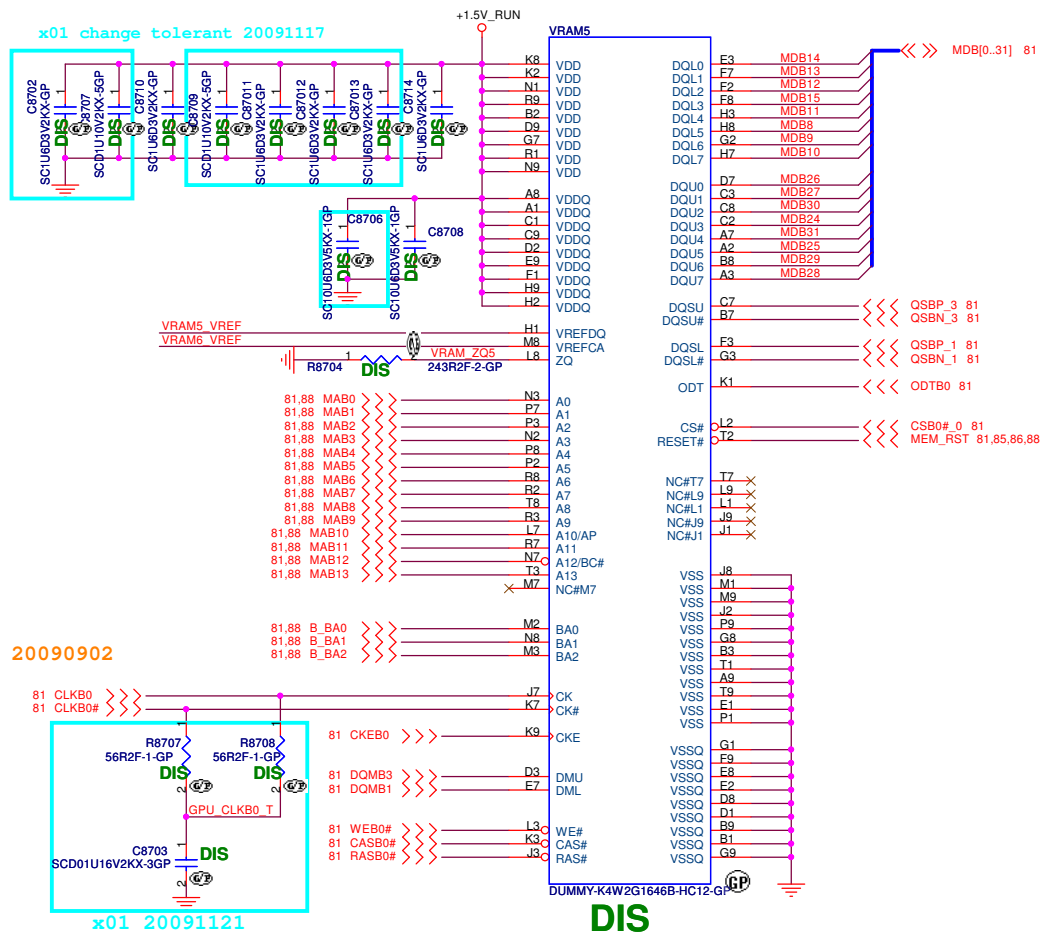
- NOTE1:**
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134
- NOTE2:**
FB_VDDC, FB_VDDCI and FB_GND are not support on M96
- NOTE3:**
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.
- NOTE4:**
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax

VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator



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Size	Document Number	Rev	
Custom	Berry	A00	
Date:	Monday, March 29, 2010	Sheet	85 of 92



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GPU-VRAM5,6 (3/4)

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Document Number

A3

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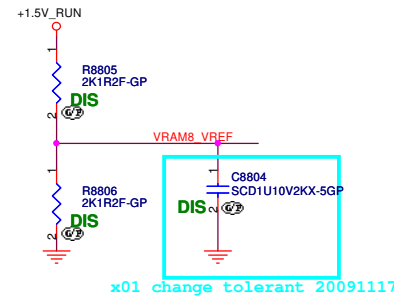
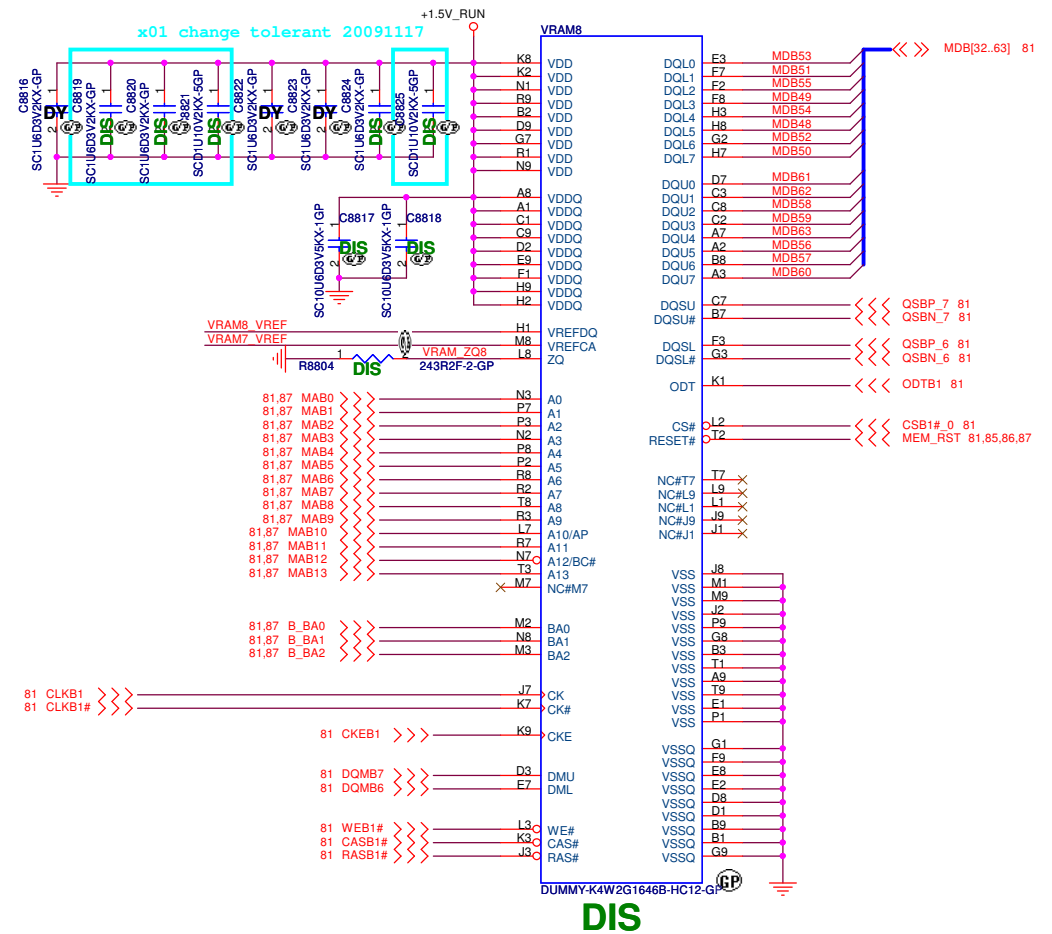
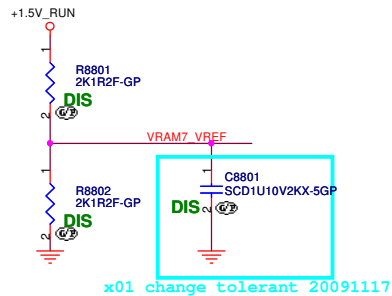
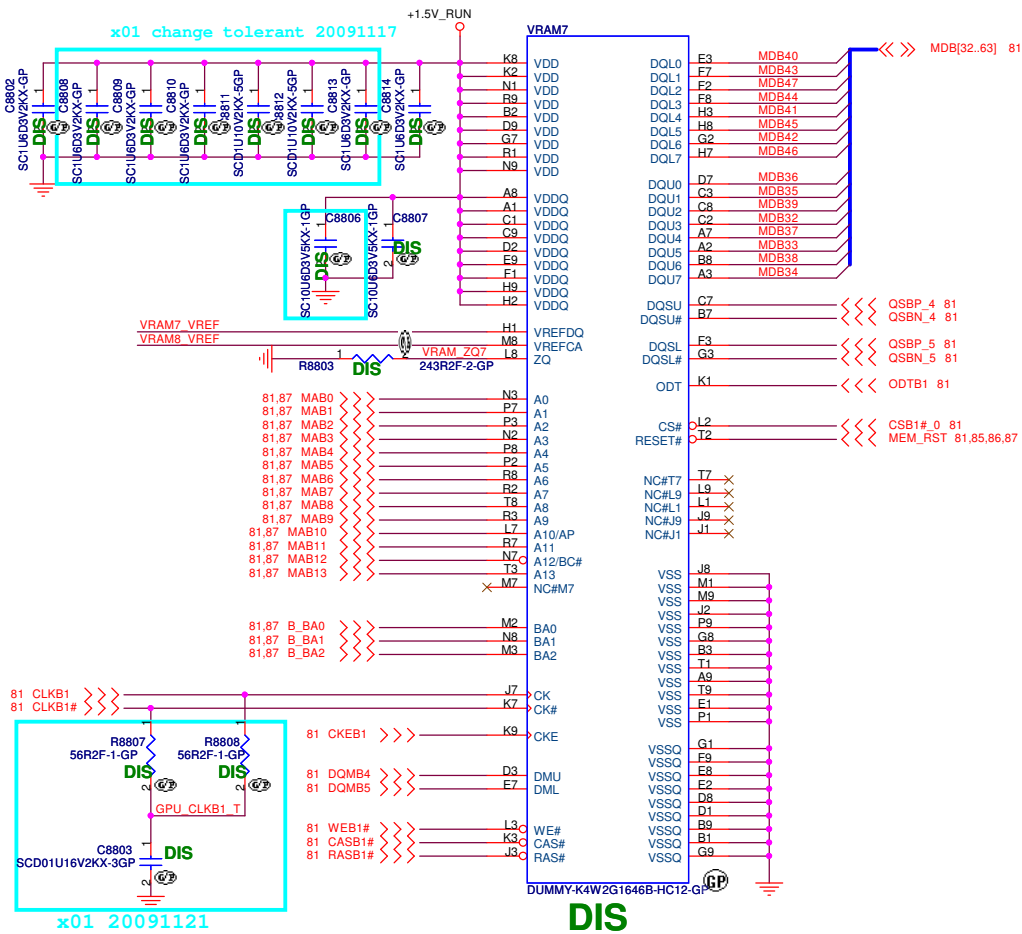
Date: Monday, March 29, 2010

Sheet 87

of

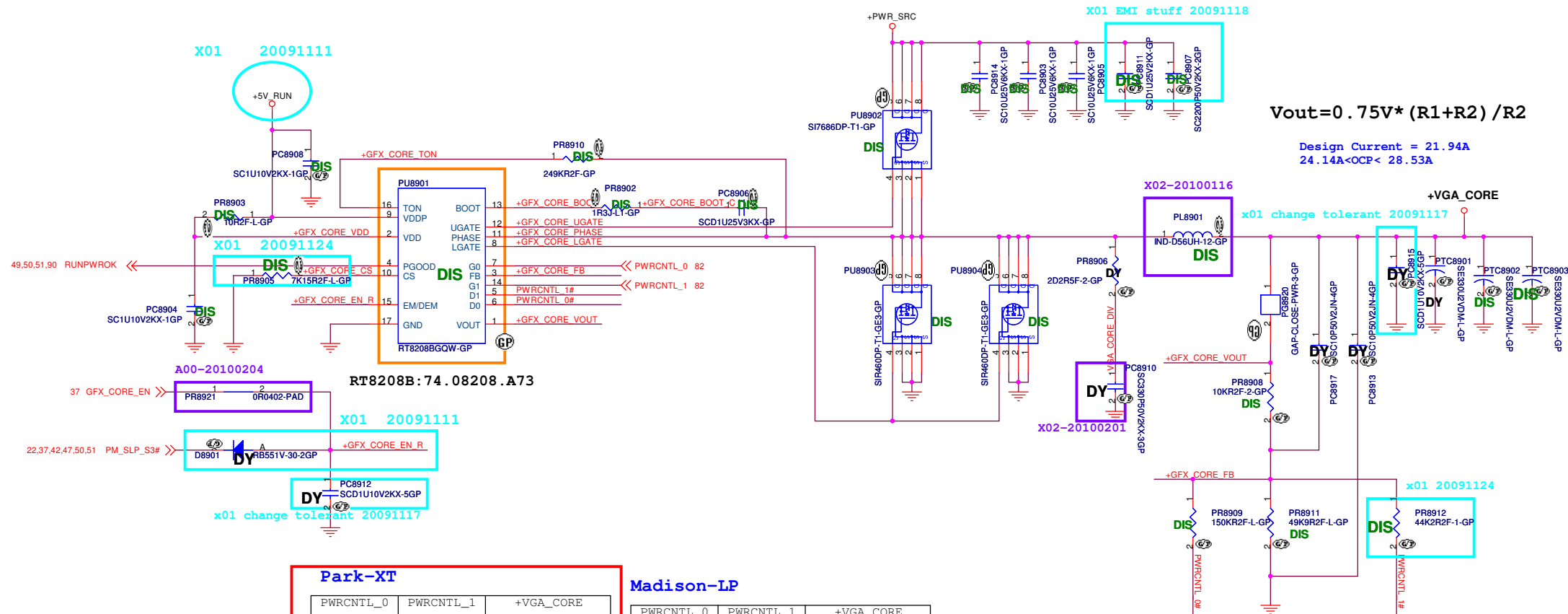
Rev

A00



SSID = Video.PWR.Regulator

RT8208BGQW for +VGA_CORE



Park-XT

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.12V

Madison-LP

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.12V

M96-LP

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.0V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SIr460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>



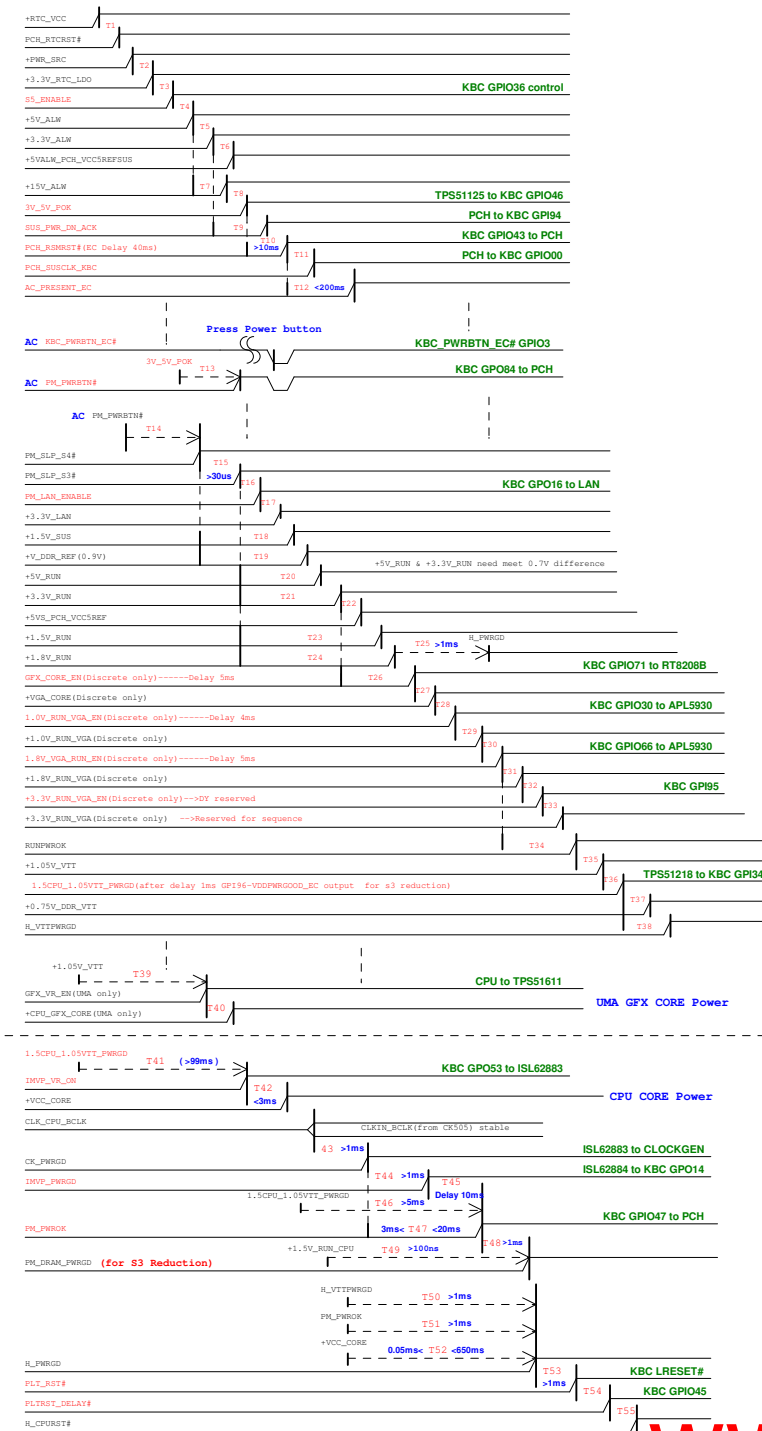
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RT8208B +VGA CORE		
Size	Document Number	Rev
A3	Arsenal DJ1 Discrete	A00
Date: Wednesday, March 31, 2010 Sheet 89 of 92		

D15 Intel-Power Up Sequence

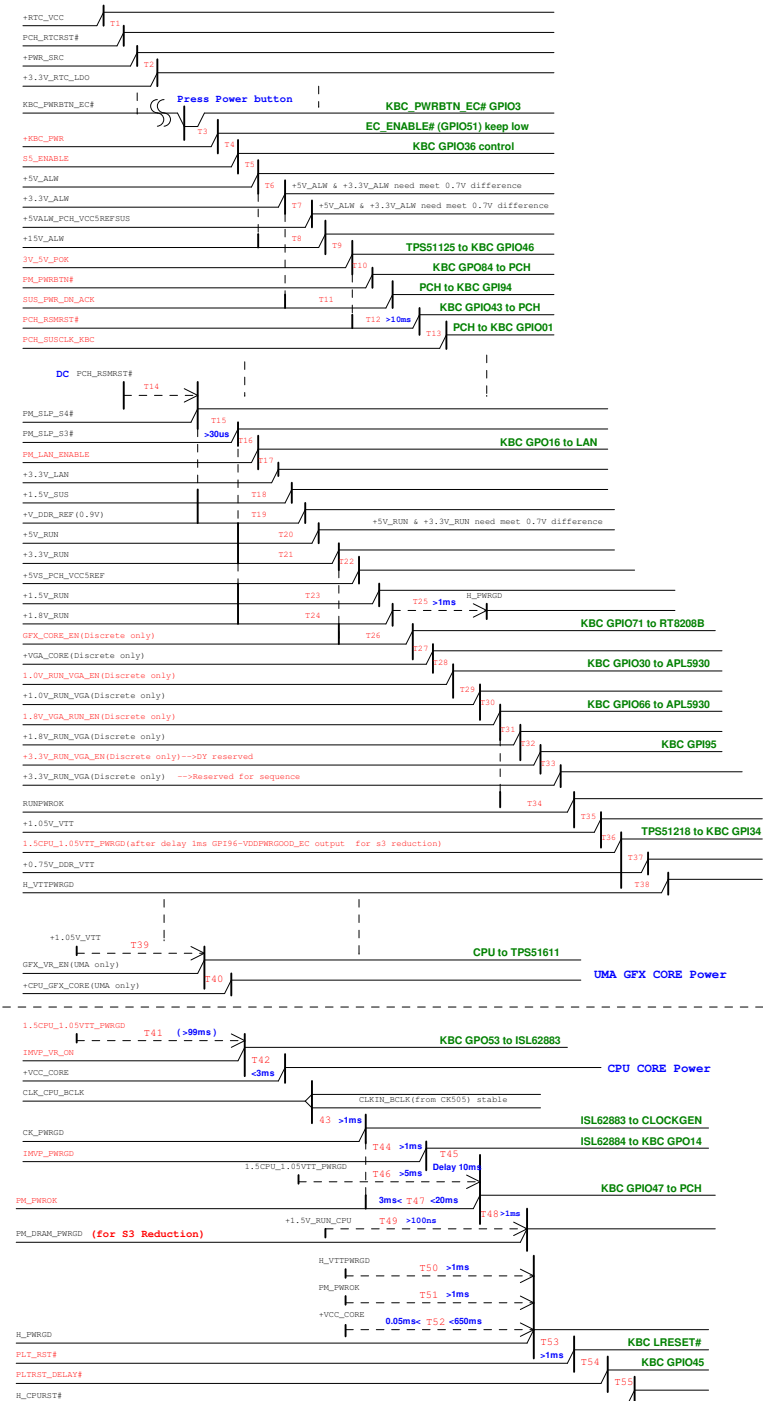
(AC mode)

red word: KBC GPIO



(DC mode)


red word: KBC GPIO



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(Blanking)

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Change History

Size	Document Number	Rev
A3	Berry	A00
Date:	Wednesday, February 10, 2010	Sheet 92 of 92